Introduction
Ferroelectric devices for memories and unconventional computing

FIXIT Teaching Module

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namlab
a tu dresden company

Funded by the European Union

Introduction – History of ferroelectric memories

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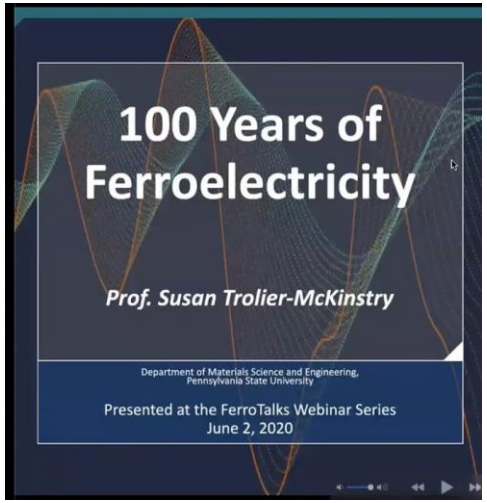
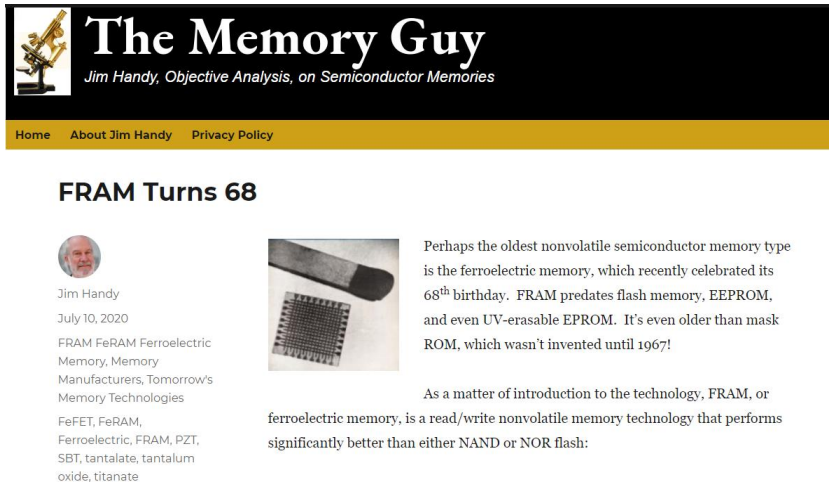
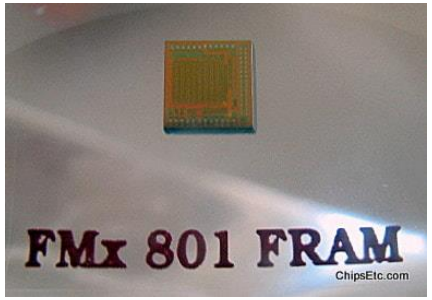
103 years of ferroelectricity



71 years of ferroelectric memory



30 years of commercial FRAM



1993
Introduction of first commercially available FRAM product 512x8 by Ramtron (now Infineon)

- Ferroelectricity in Rochelle salt has been discovered 103 years ago by Josef Valasek
- Ferroelectric memories have been invented 71 years by Dudley Allen Buck
- FRAM is commercially available since 30 years. First products were offered by Ramtron

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Introduction – First report of ferroelectric hafnium oxide

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12 years of ferroelectric hafnia

Home > Applied Physics Letters > Volume 99, Issue 10 > 10.1063/1.3634052

Full . Published Online: 08 September 2011 Accepted: August 2011

Ferroelectricity in hafnium oxide thin films

Appl. Phys. Lett. **99**, 102903 (2011); https://doi.org/10.1063/1.3634052

T. S. Böscke[1, a),b)], . Müller[2], D. Bräuhaus[3], U. Schröder[4, b)], *and* U. Böttger[3]

Full • Submitted: 26 July 2011 • Accepted: 14 August 2011 • Published Online: 12 September 2011

Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications

Home > Journal of Applied Physics > Volume 110, Issue 11 > 10.1063/1.3667205

Full • Submitted: 23 September 2011 • Accepted: 05 November 2011 • Published Online: 07 December 2011

Ferroelectricity in yttrium-doped hafnium oxide

Journal of Applied Physics **110**, 114113 (2011); https://doi.org/10.1063/1.3667205

J. Müller[1, a)], U. Schröder[2, b)], T. S. Böscke[3, b)], I. Müller[4], U. Böttger[4], L. Wilde[1], J. Sundqvist[1, b)], M. Lemberger[5], P. Kücher[1], T. Mikolajick[2,6], *and* L. Frey[5,7]

View Affiliations View Contributors

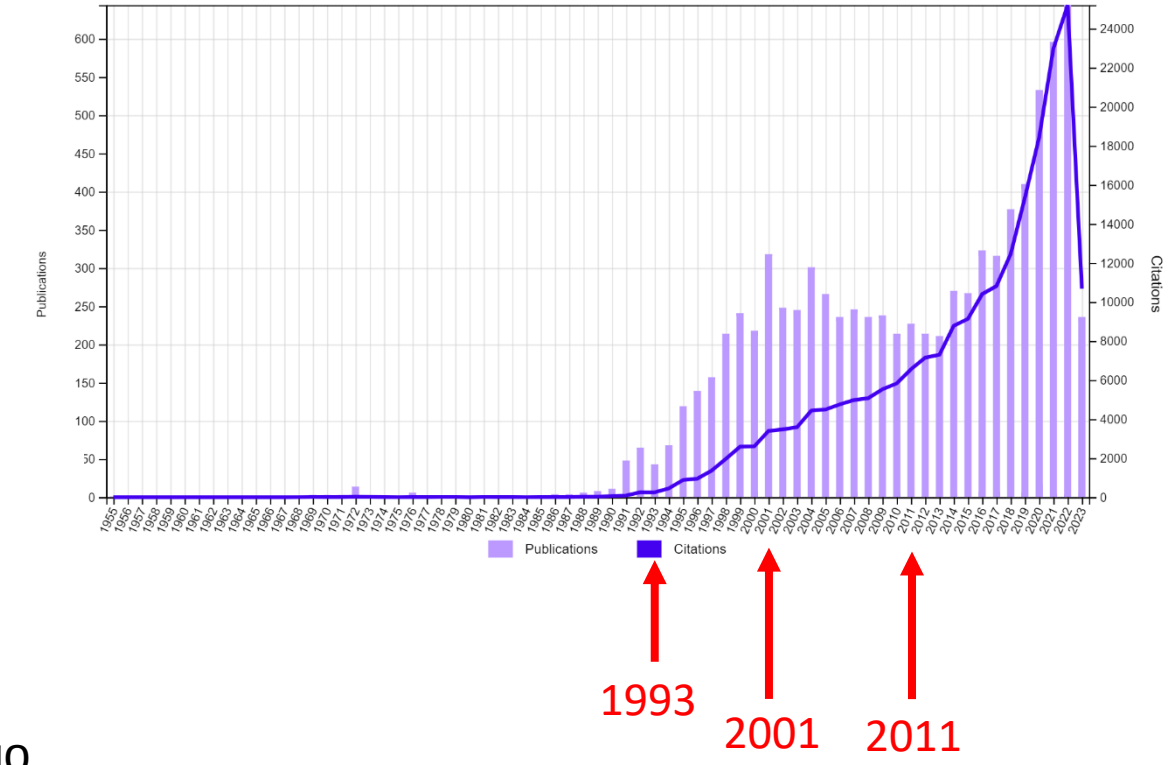
4 years of ferroelectric AlScN

AlScN: A III-V semiconductor based ferroelectric

Cite as: J. Appl. Phys. **125**, 114103 (2019); doi: 10.1063/1.5084945
Submitted: 7 December 2018 · Accepted: 28 February 2019 ·
Published Online: 18 March 2019

Simon Fichtner,[1,2] Niklas Wolff,[3] Fabian Lofink,[2] Lorenz Kienle,[3] and Bernhard Wagner[1,2]

Publications and citations on the topic "ferroelectric memories"



- Ferroelectric hafnium oxide was reported 12 years ago
- Research activities have reached new heights by having a CMOS compatible ferroelectric at hands
- Ferroelectric AlScN was reported only 4 years ago

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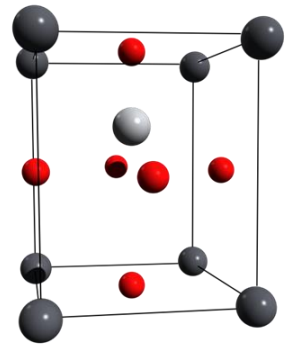
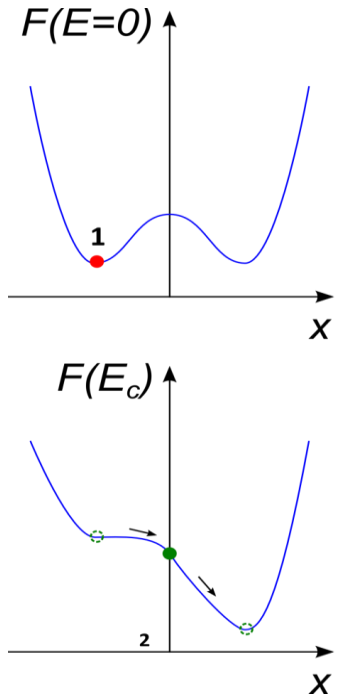
Ferroelectric crystal



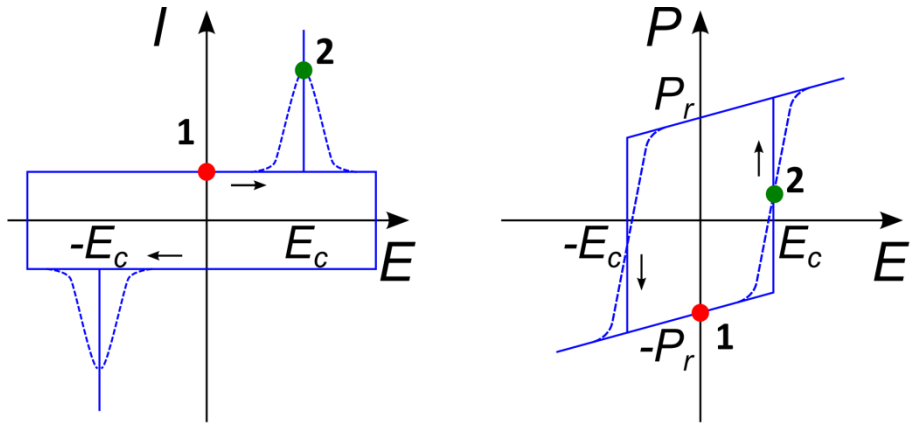
tetragonal ($T < T_C$)

Double well potential of ferroelectric material



Hysteresis

$$P = \frac{1}{A}\int I\,(t)\,dt$$



■ Ferroelectrics have two stable polarization states that can be switched by applying an electric field
→ **no inefficiency** during writing → **lowest write energy** of known nonvolatile concepts

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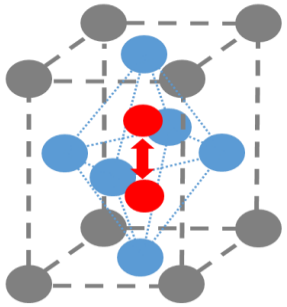
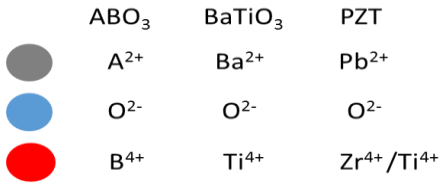
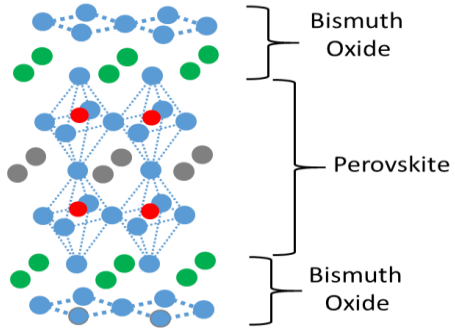
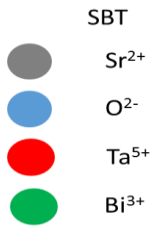
Lead-Zirconium Titanate (PZT)



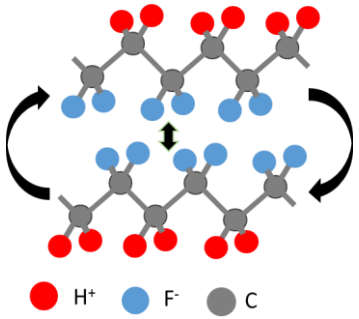


Strontium-Bismuth-Tantalate (SBT)

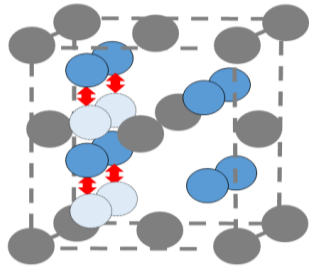


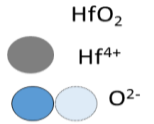


Polyvinylidenfluoride (PVDF)

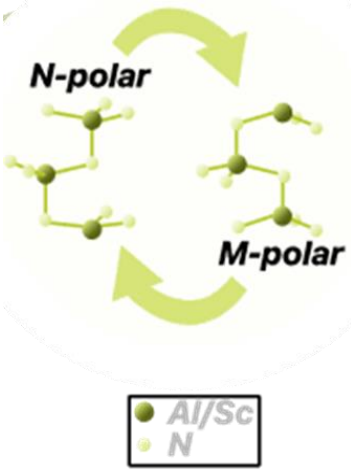


Orthorhombic Hafnium Oxide (X:HfO_2)





Aluminum Scandium Nitride (AlScN)



U. Schröder et al., Nature Reviews Materials 2022

T. Mikolajick et al., IEDM 2019, TED 2020, JAP 2021

$2P_R$	~ 30-60µC/cm²	~ 15-30µC/cm²	~ 10-15µC/cm²	~ 30-80µC/cm²	~ 150-250µC/cm²
E_C	~ 0.1 MV/cm	~ 0.05 MV/cm	~ 0.5 MV/cm	~ 1-2 MV/cm	~ 2-5 MV/cm
k	~ 300 – 600	~ 200 – 300	~ 10	~ 30	~ 25
CMOS Comp.	Low to **Medium**	**Low** to Medium	very Low	High	Medium to High Ideal fit to GaN HEMT

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- Introduction
- **Ferroelectric memory devices**
  - Ferroelectric capacitor - FeCAP (for FeRAM)
  - Ferroelectric Field Effect Transistor - FeFET
  - Ferroelectric Tunneling Junction - FTJ
- Ferroelectrics for unconventional computing
- Ferroelectric device comparison
- Conclusion

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Benefits of Ferroelectric HfO_2

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- HfO_2 is a simple binary oxide

  ➔ **various mature deposition techniques**

- Well known high-k material in semiconductor industry

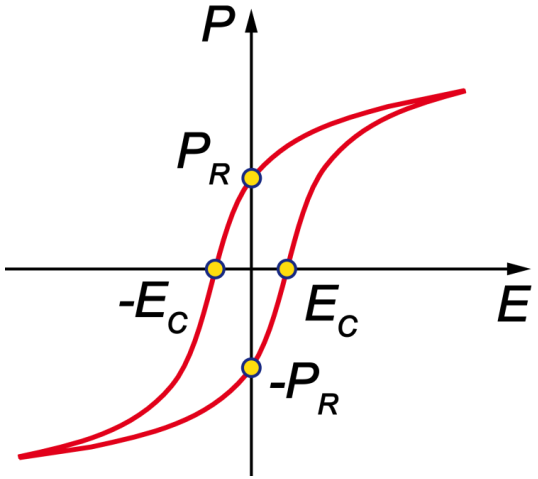
  ➔ **CMOS compatible**

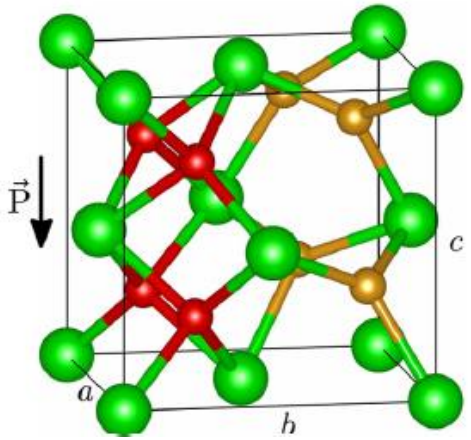
- Robust ferroelectricity even upon

  ➔ **aggressive vertical and lateral scaling**

- Large bandgap (5.3-5.7 eV)

  ➔ **reduced leakage**





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Three ferroelectric memory elements

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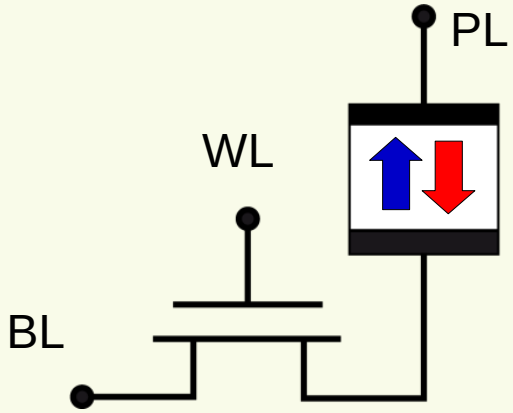
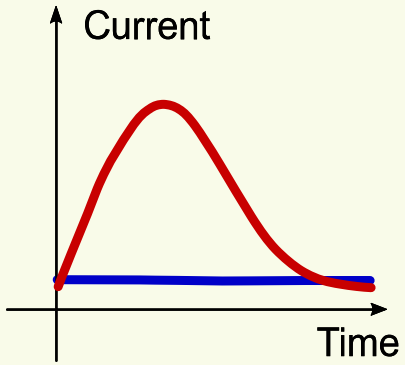
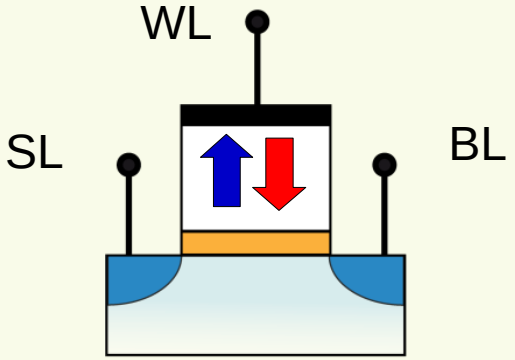
FeCAP



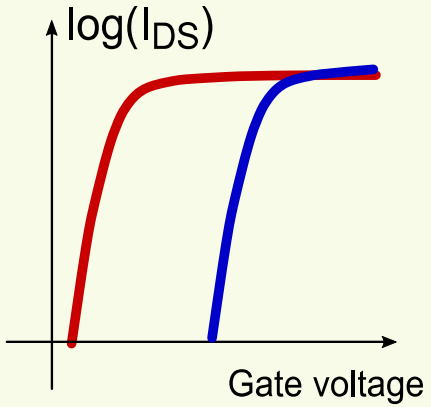
Ferroelectric displacement current



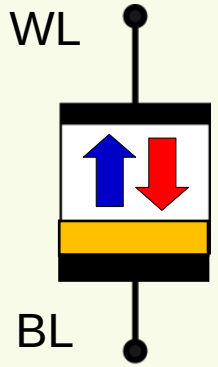
FeFET



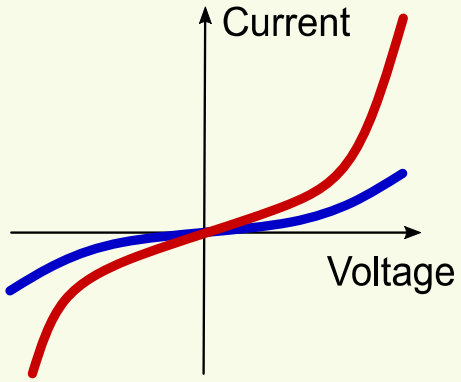
V_T shift due to polarization charges



FTJ



Polarization-dependent tunneling current



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Three ferroelectric memory elements

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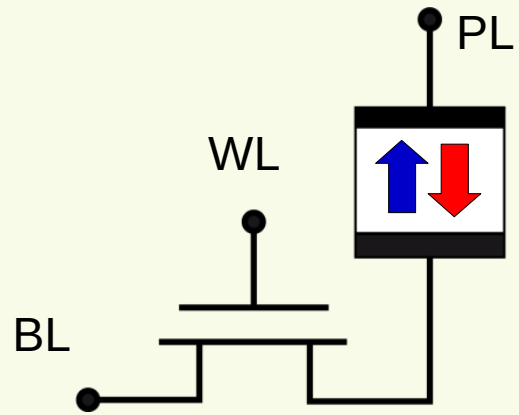
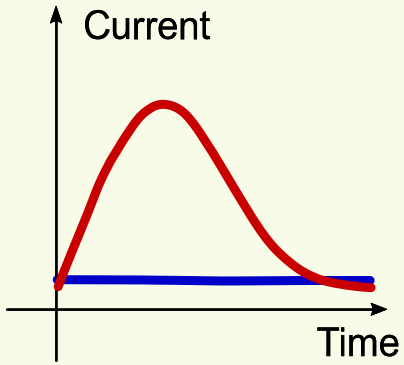
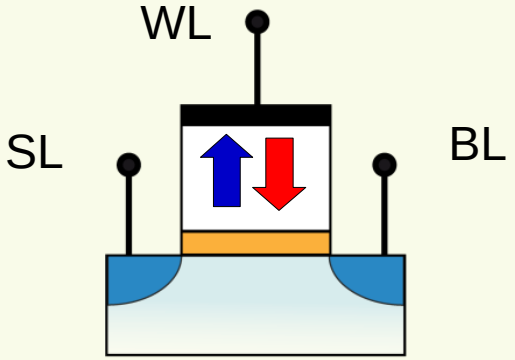
FeCAP



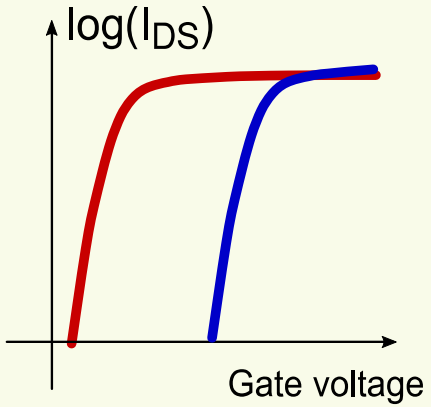
Ferroelectric displacement current



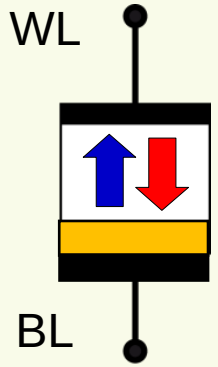
FeFET



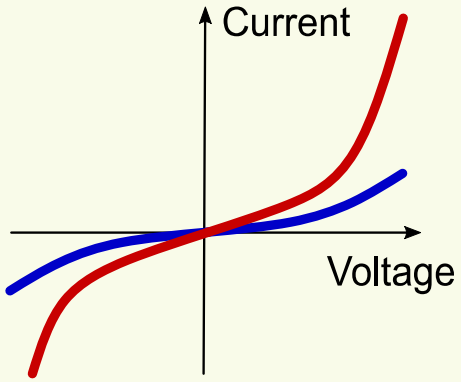
V_T shift due to polarization charges



FTJ



Polarization-dependent tunneling current



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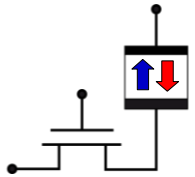
Basic Ferroelectric Memory Devices – FeCAP for FeRAM



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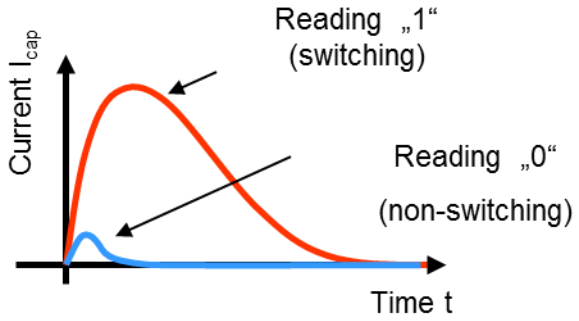
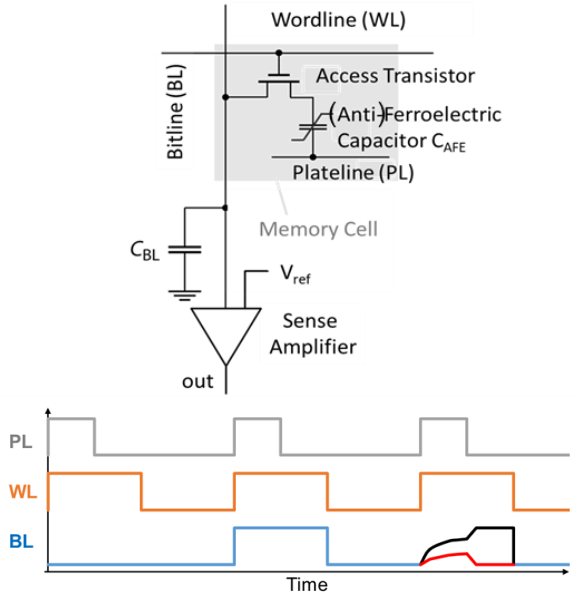
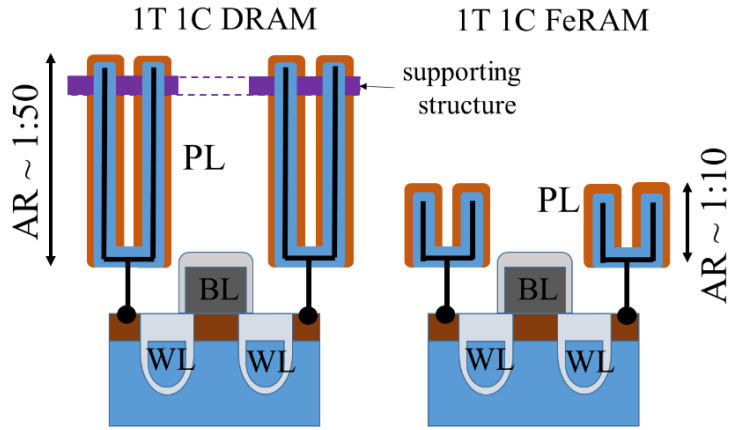
Curent reponse during reading out of a capacitor



Readout in 1T-1C FeRAM cell



Comparison of stacked capacitor height between DRAM and HfO_2 based FeRAM

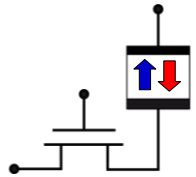


S. Slesazeck et al. IWCM2 2018

- For readout a pulse in a defined direction is applied to the capacitor
- If the ferroelectric does not switch then only the displacement current will flow
- If the ferroelectric switches, then in addition to the displacement current the switching current will flow
- Switched charge needs to be high enough to develop a reasonable voltage on the bitline

Funded by the European Union

Basic Ferroelectric Memory Devices – FeCAP for FeRAM



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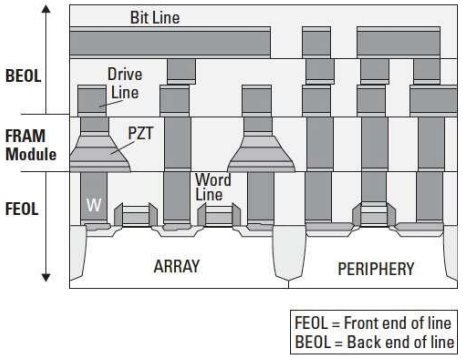
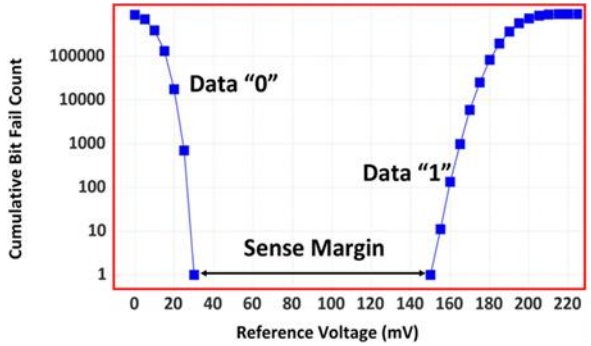
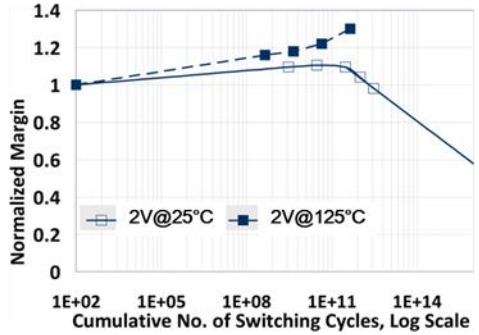
Schematic cross section of 130nm PZT FeRAM



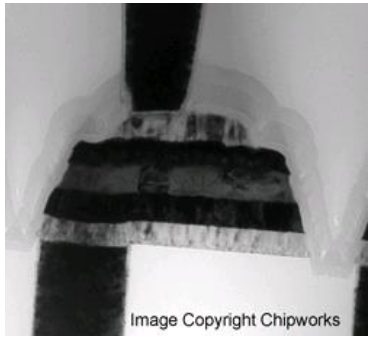
Bit distribution for 180nm PZT FeRAM chip in 2T-2C mode



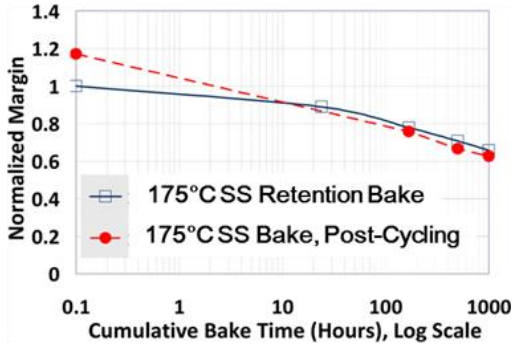
Enduracnce of 180nm PZT FeRAM chip in 2T-2C mode



TEM Cross section of PZT FeRAM capacitor



Retention test for 180nm FeRAM chip in 2T-2C mode with and without pre-cycling



- First ferroelectric memories came to market in the early 1990s
- Today state of the art is 130nm/90nm technology
- Very good performance and reliability data

K. R. Udayakumar et al., IMW 2013

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Basic Ferroelectric Memory Devices – FeCAP for FeRAM

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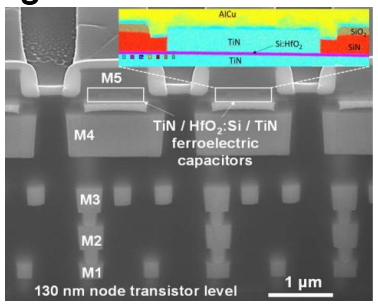
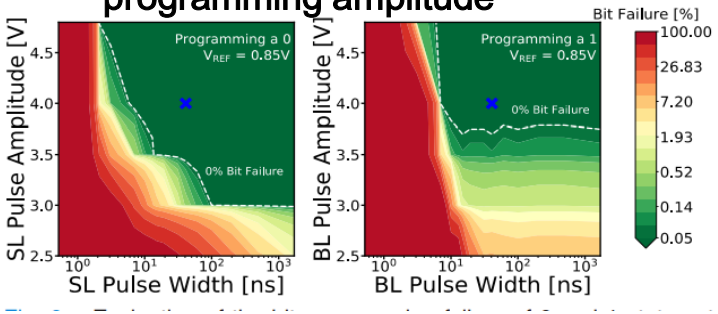
SEM of HZO based FeRAM cells integrated in 130nm CMOS



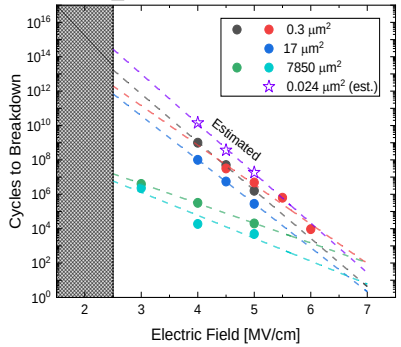
Bit failures as a function of programming amplitude



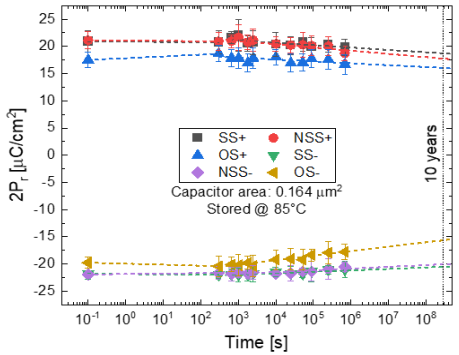
T. Francois et al., IEDM 2019, 2021

T. Francois et al., TED 2022

Field dependent Endurance of MFM capacitor with Si-doped HfO_2 for different capacitor sizes

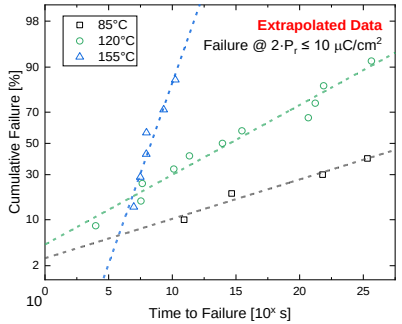


Retention of MFM capacitor with Si-doped HfO_2 for different capacitor sizes



R. Alcala et al., EDTM 2022

Extrapolated retention failure rate for different temperatures



Influence of area, Temp and Field on reliability of MFM capacitor with Si-doped HfO_2

	Wake-Up	Cycles to Break.	Imprint	Retention
Area (↓)	-	↑	-	-
Temperature (↓)			↓	↑
Electric Field (↓)	-	↑		

R. Alcala et al., JEDS 2022

■ Promising data for integrated FeRAM using silicon doped hafnium oxide has been shown

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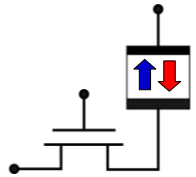
Basic Ferroelectric Memory Devices – FeCAP for FeRAM



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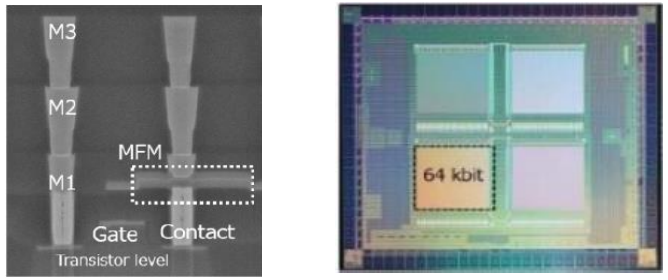
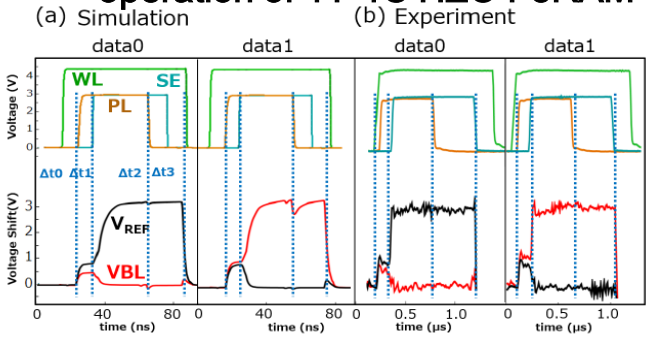
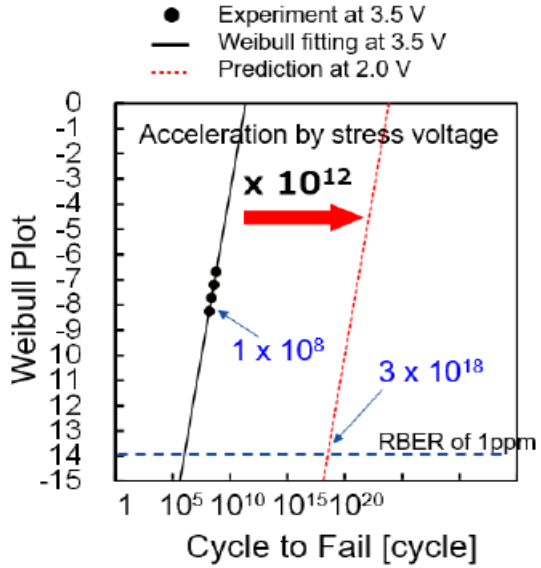
Cross section of cell and top view of 64kbit 1T-1C HZO FeRAM



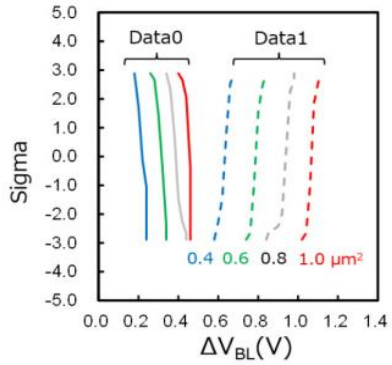
Simulated and measured read operation of 1T-1C HZO FeRAM



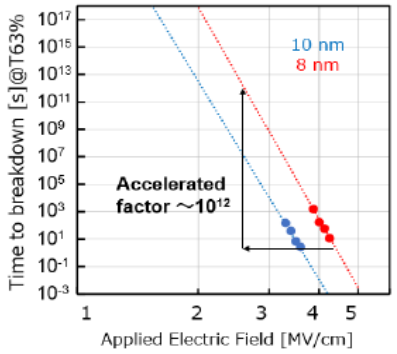
Weibull plot of the cycling failures measured and extrapolated for a 8nm thick HZO film



V_{BL} distribution of 1T1C HZO FeRAM for different capacitor sizes



Time to breakdown for HZO as a function of electric field and film thickness

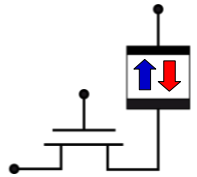


J. Okuno et al., VLSI 2020 | J. Okuno et al., JEDS | J. Okuno et al., EDTM

- First promising data for integrated FeRAM using HZO has been shown

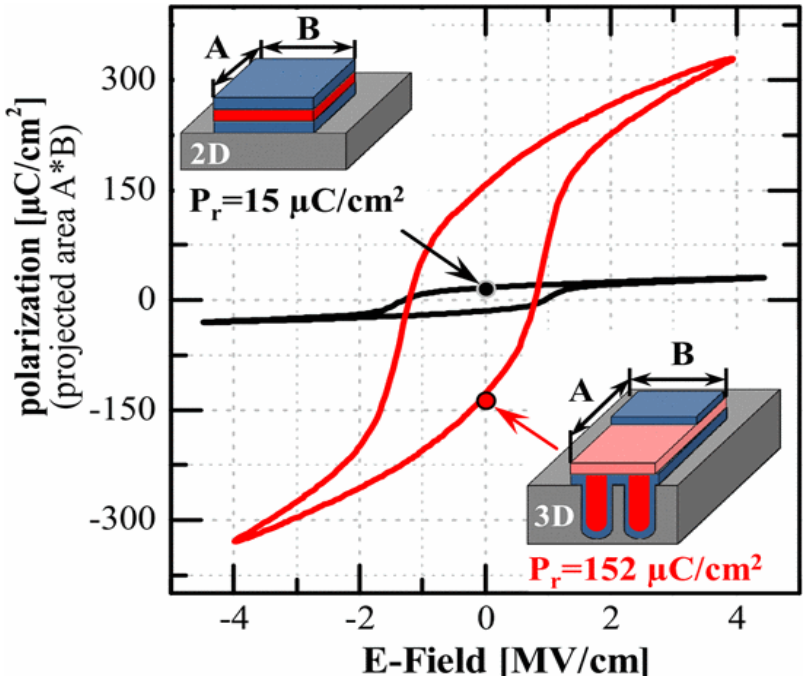
Funded by the European Union

Basic Ferroelectric Memory Devices – FeCAP for FeRAM



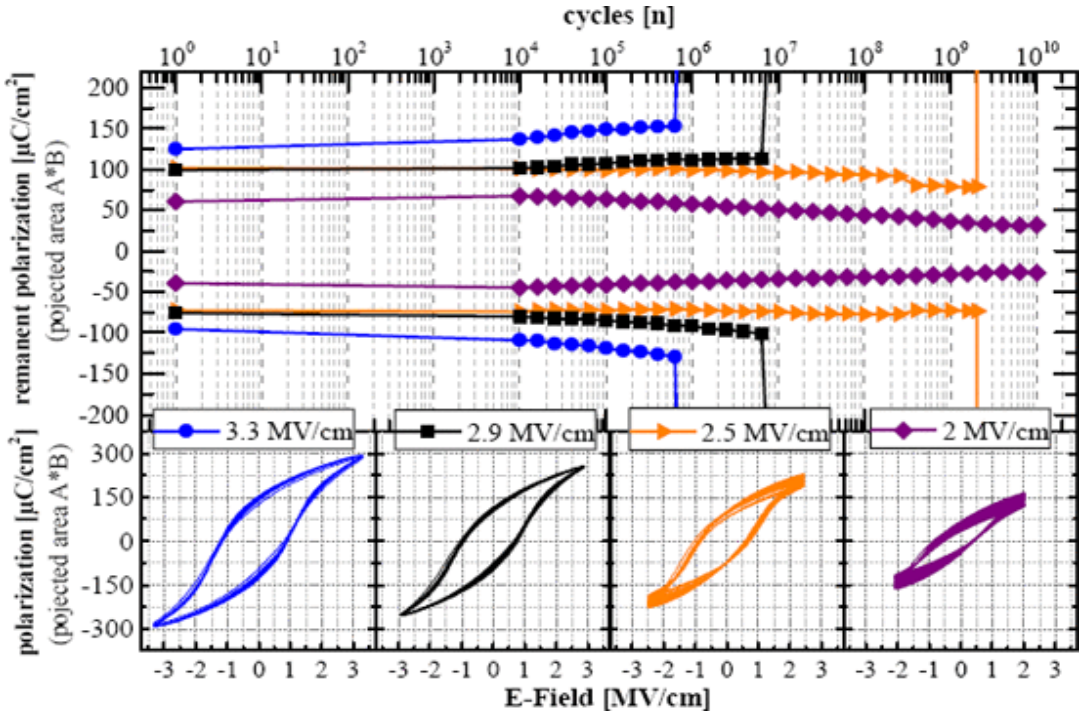
FIXIT

Polarization per footprint of 2D and 3D structure



J. Müller et al., IEDM 2013

Endurance of 3D structures for different cycling fields

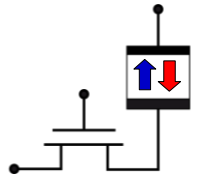


P. Polakowski, IMW 2014

- 3D integration is straight forward based on available ALD processes

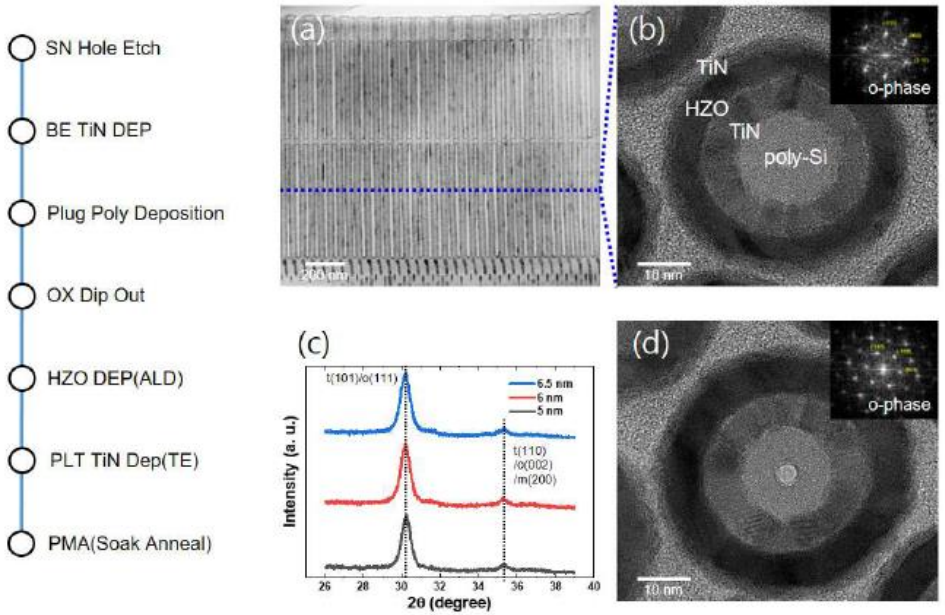
Funded by the European Union

Basic Ferroelectric Memory Devices – FeCAP for FeRAM

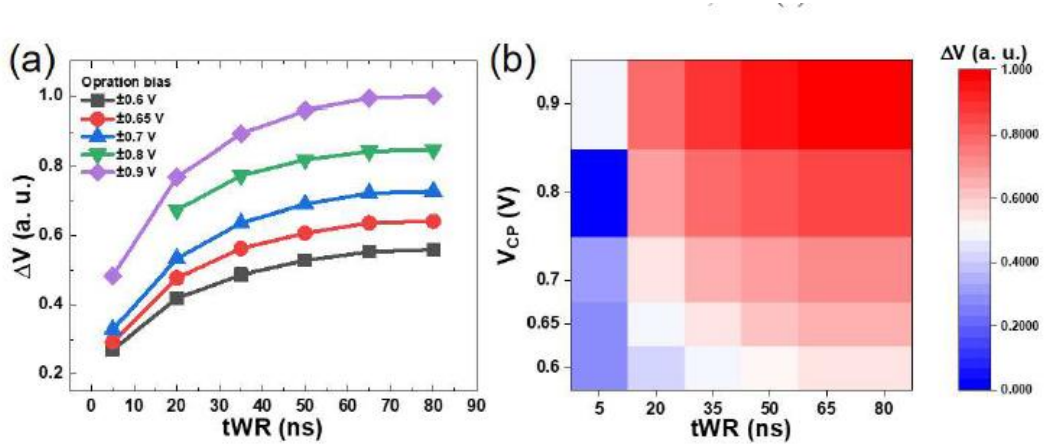


FIXIT

Process flow, cross vertical and top-view cross sections as well as XRD pattern for 5nm and 7nm HZO integrated into 1xnm technology



Characterization of writing process in 1xnm HZO based FeRAM



- First demonstration of HZO integration into 1xnm technology
- Little data publicly available so far

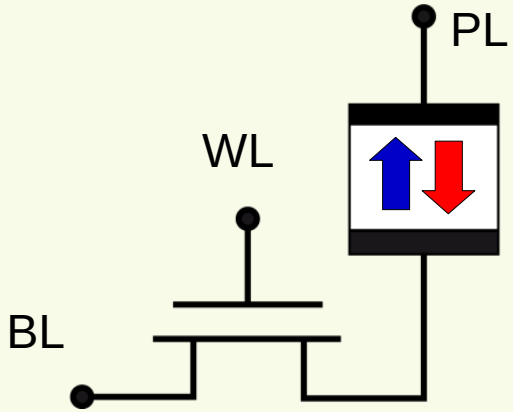
M. Sung et al., IEDM 2021

Funded by the European Union

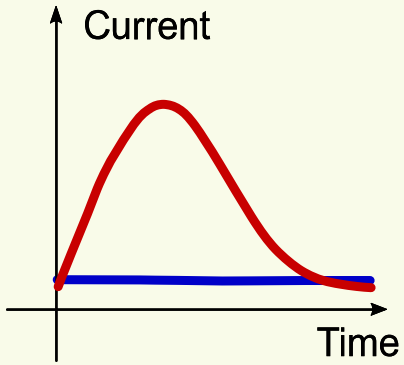
Three ferroelectric memory elements

FIXIT

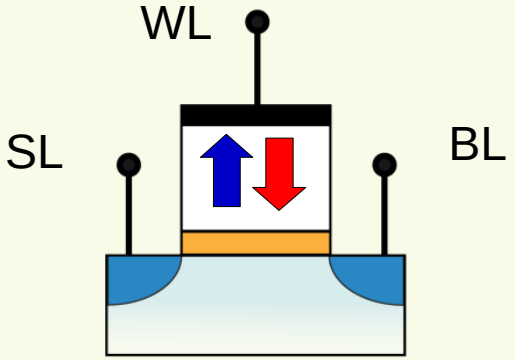
FeCAP



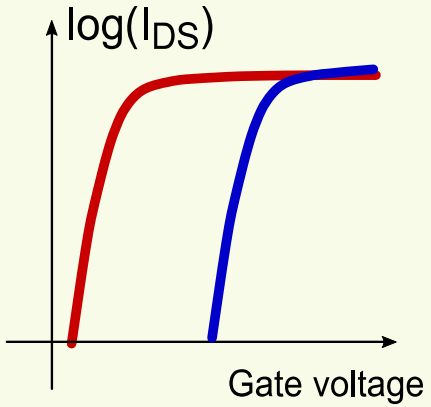
Ferroelectric displacement current



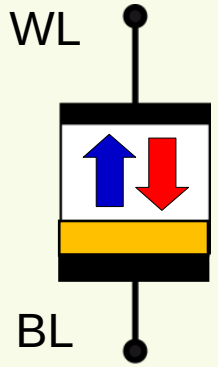
FeFET



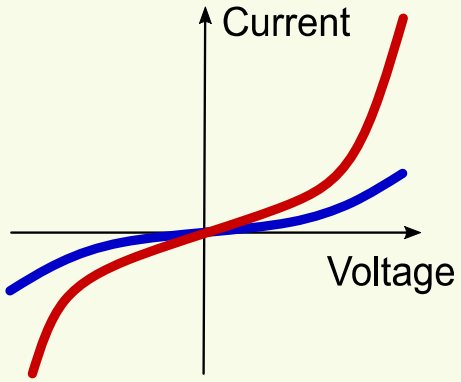
V_T shift due to polarization charges



FTJ

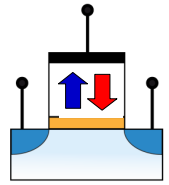


Polarization-dependent tunneling current



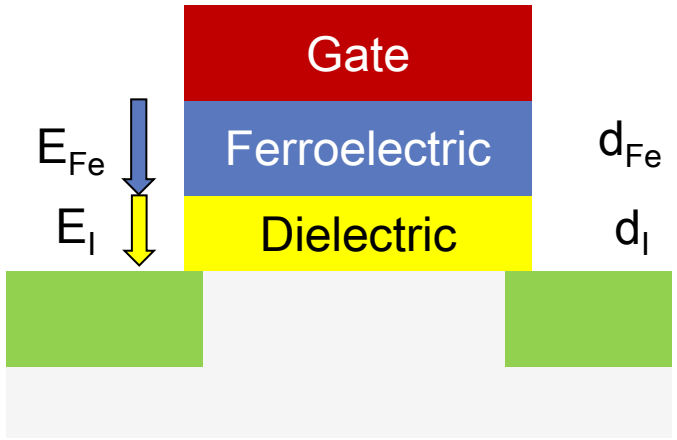
Funded by the European Union

FeFET – Operation principle



FIXIT

Generic ferroelectric FET



Gate voltage

$$V_G = \varphi_S + \frac{Q_{sc}(\varphi_S)}{C_{Stack}} + E_{Fe} \cdot d_{Fe}$$

At flatband

$$V_{FB} = E_{Fe}(P = 0) \cdot d_{Fe}$$

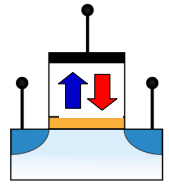
Memory window

$$MW = V_{FB+} - V_{FB-} \approx 2 \cdot E_C \cdot d_{Fe}$$

- Qsc is the space charge in the silicon and C_{stack} is the capacitance of the series connection of ferroelectric and dielectric capacitor (assumption: No trapped or fixed charge)
- The nonlinear and switching behavior of the ferroelectric as a function of the electrical field modifies the I-V characteristics of a FeFET compared to a normal MOSFET
- The ferroelectric switching leads to hysteresis
- The memory window depends on the coercive field and the thickness of the material

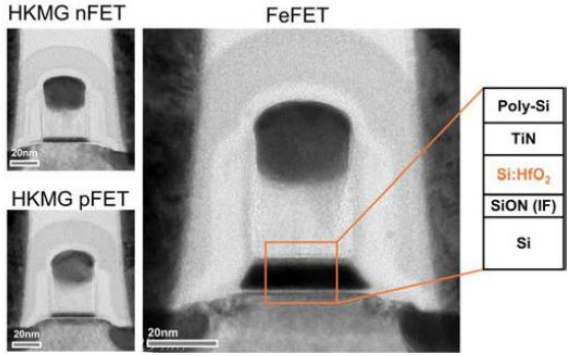
Funded by the European Union

Si FeFET – State-of-the-art

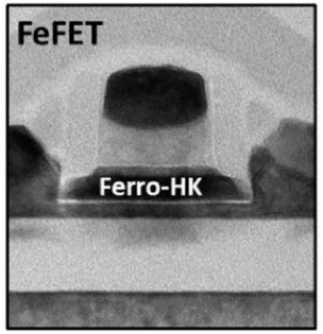


FIXIT

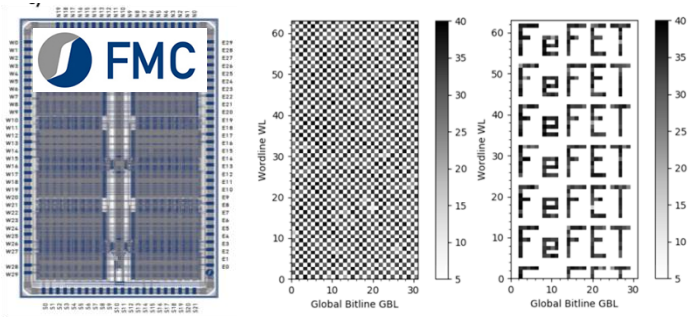
Cross sections of 28nm logic FETs and FeFET



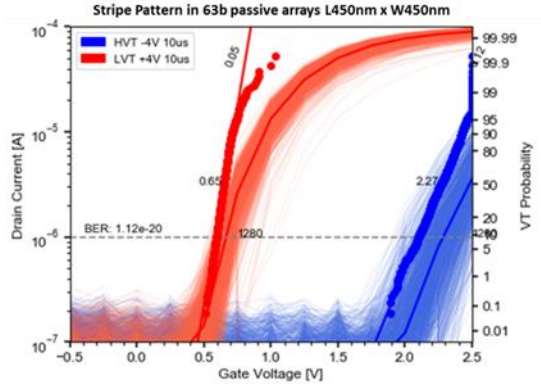
22nm FDSOI FeFET device



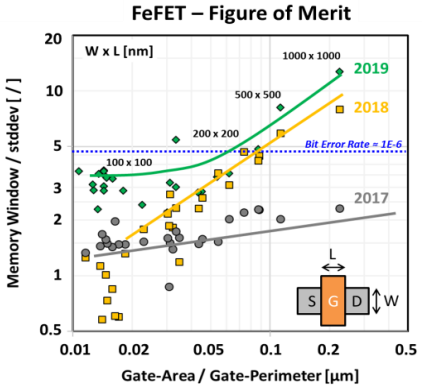
10MbArray
Layout and test patterns



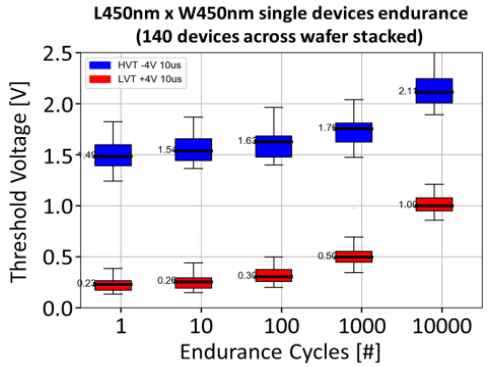
I-V curves for low and high VT states of 28nm FeFET device across wafer



Improvement of Variability over time



Cycling endurance behavior



M. Trentzsch et al., IEDM 2016

S. Dünkel et al., IEDM 2017

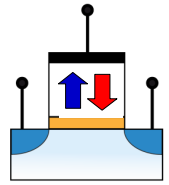
S. Beyer et al., IMW 2020

- Cell transistor only differs in HfO_2 details; Periphery devices not affected
- Array is fully functional and variability is continuously improving

H. Mulasomanovic et al., Nanotechnology 2021

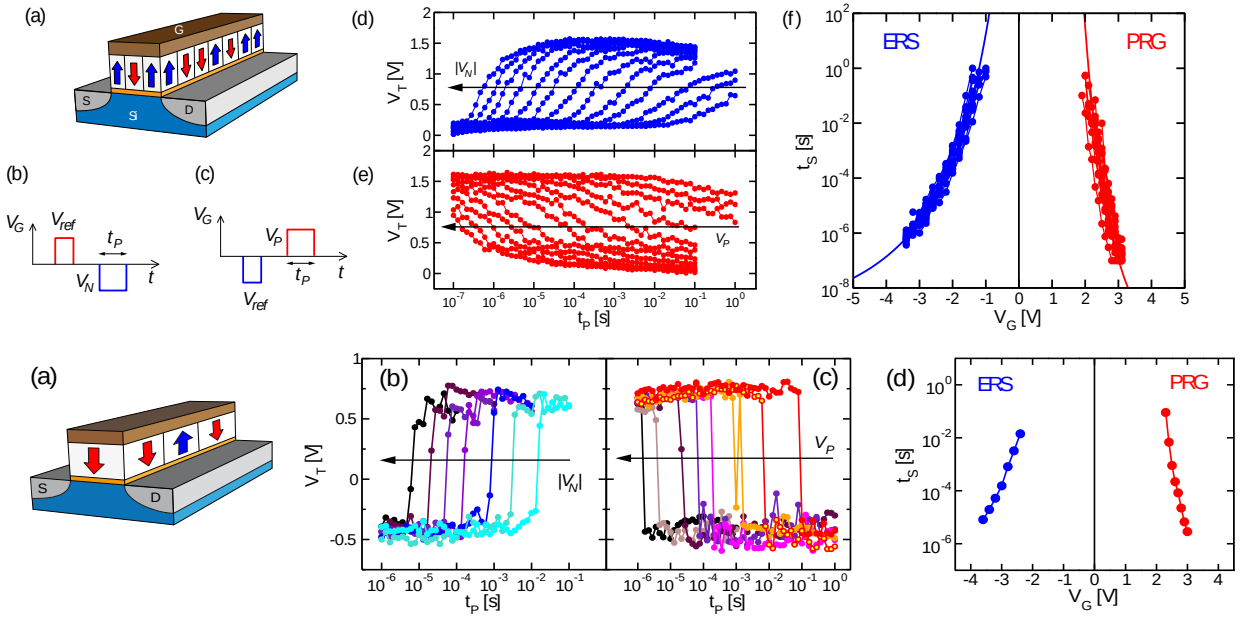
Funded by the European Union

FeFET switching kinetics

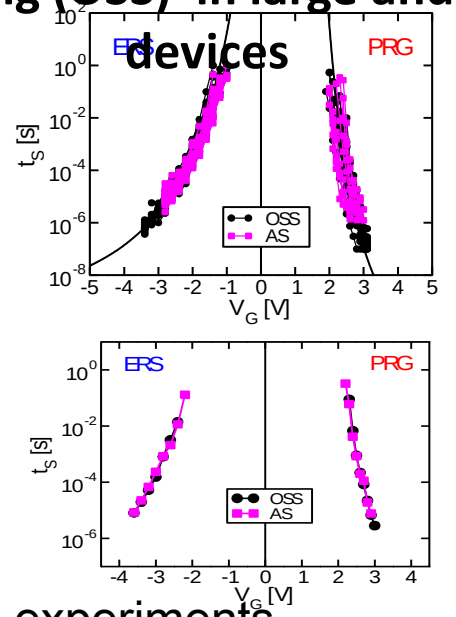


FIXIT

Construction of VG vs. ts plots using one shot switching in large and small devices



Comparison of accumulative switching (AS) and one shot switching (OSS) in large and small devices

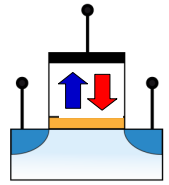


- VG vs. t_s plot can be used to extract retention behavior form switching experiments
- Switching in large and small devices is continuous vs. abrupt
- VG vs. t_s behavior is universal for large and small devices using one shot and accumulative switching

H. Mulaosmanovic et al., TED 2020

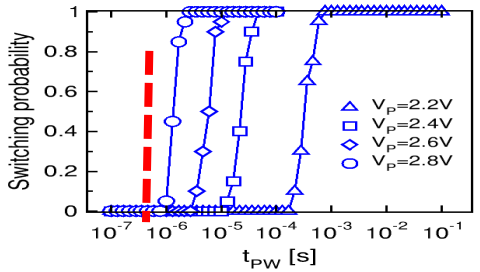
Funded by the European Union

Single-Domain FeFET - Switching probability

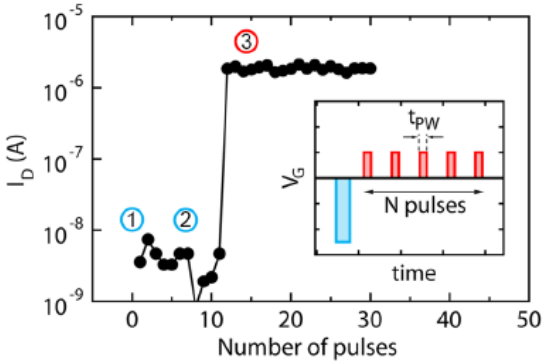


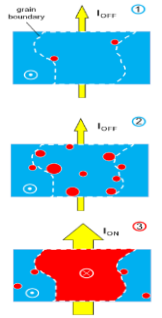
FIXIT

Switching probability of scaled (80nm/20nm) FeFET

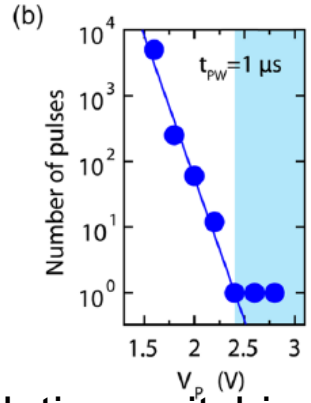


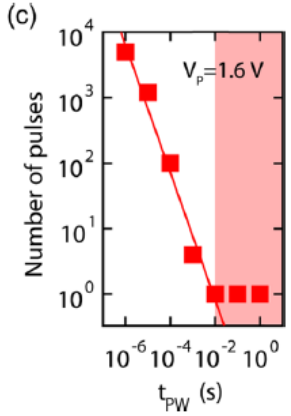
Accumulative switching of scaled FeFET





Number of pulses required to switch scaled FeFET as a function of pulse height and width





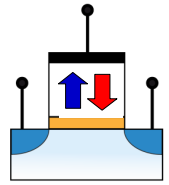
- Ultra-scaled FeFETs exhibit accumulative switching
- Probability curve is tunable
- The effect can be used for mimicking biological neurons

H. Mulaosmanovic et al., ACS AMI 2018

H. Mulaosmanovic et al., Nanoscale 2018

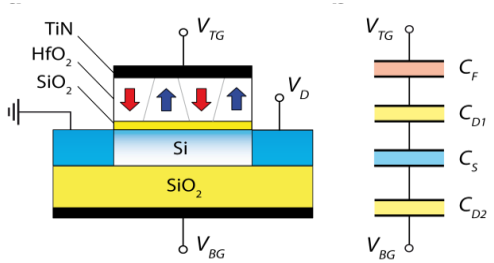
Funded by the European Union

Ferroelectric Memories – FeFET

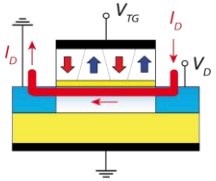


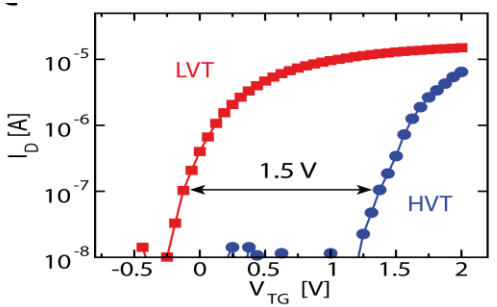
FIXIT

FDSOI FeFET illustrating front- and back-gate capacitances

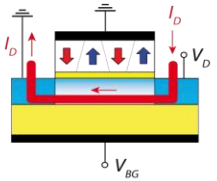


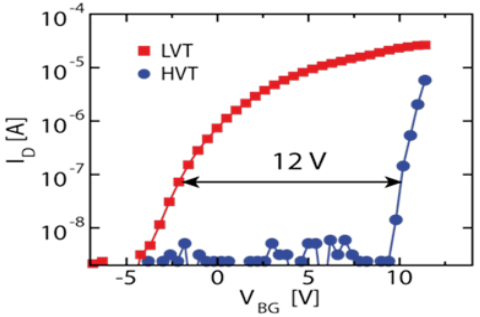
Reading from front-gate



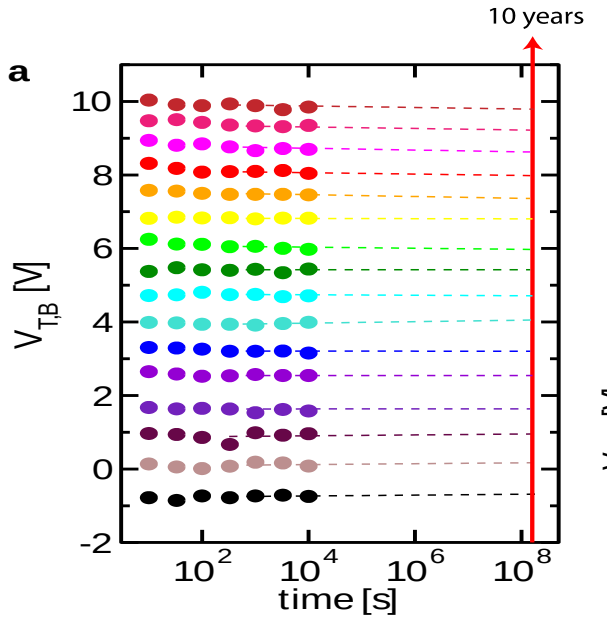


Reading from back-gate





Demonstration of 8-V_T levels

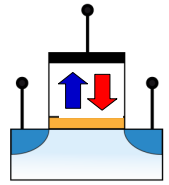


H. Mulaosmanovic et al., Nanoscale 2021

- With two different gates, the write and read paths of a FeFET can be decoupled
- With a significantly thicker gate dielectric in between second gate and channel, the read signal is amplified
- One possible implementation can be achieved by using the back-gate of an FDSOI device

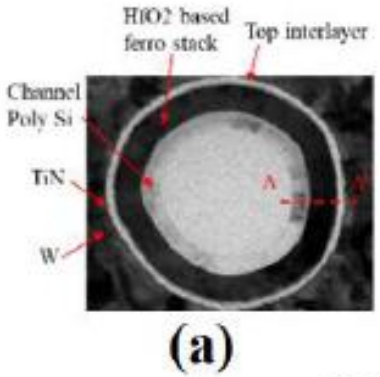
Funded by the European Union

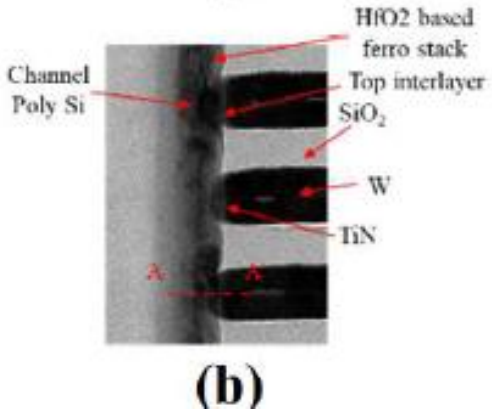
MLC in FeFETs



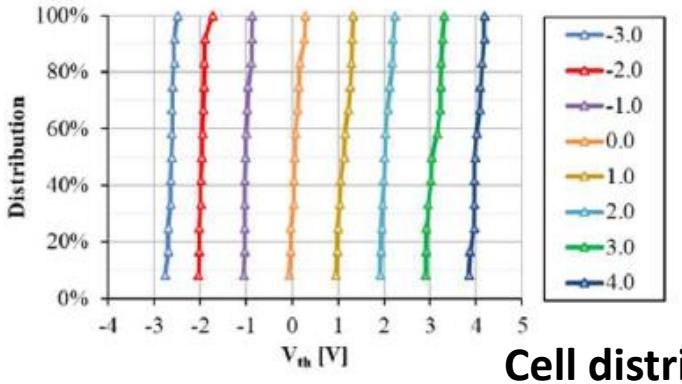
FIXIT

FeFET integrated into 3D NAND

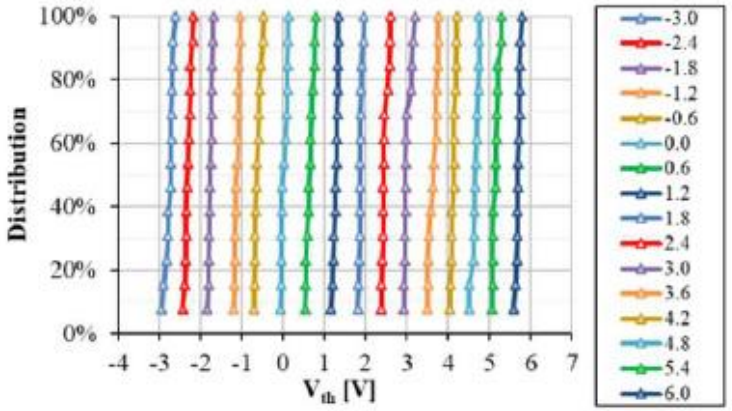




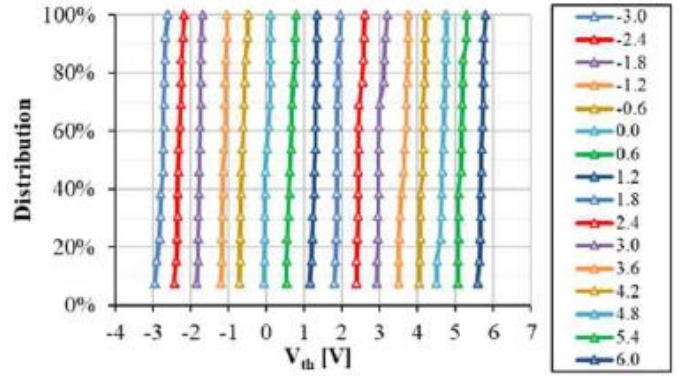
Cell distributions for 3bits per cell



Cell distributions for 4bits per cell



Cell distributions for 4 bits per cell after 3k cycles



- First data on integration of ferroelectric Hafnia into 3D NAND shows promising data even for 3 - 4 bits/cell operation

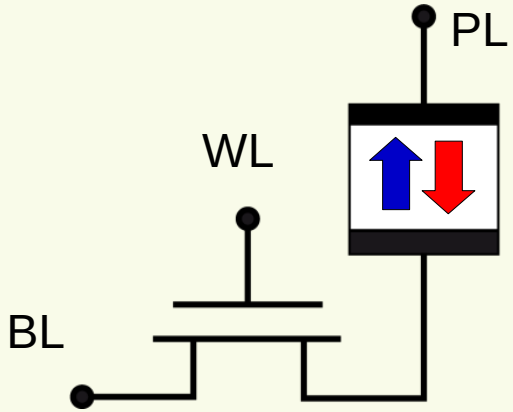
S. Yoon et al. , VLSI 2023

Funded by the European Union

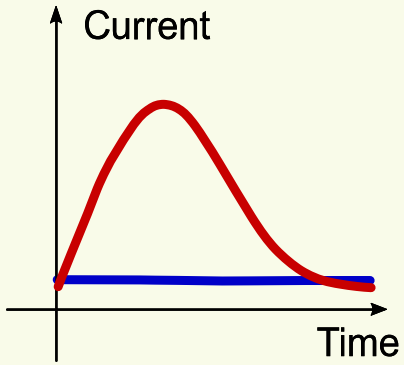
Three ferroelectric memory elements

FIXIT

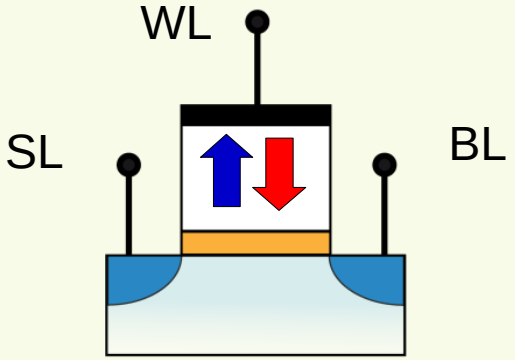
FeCAP



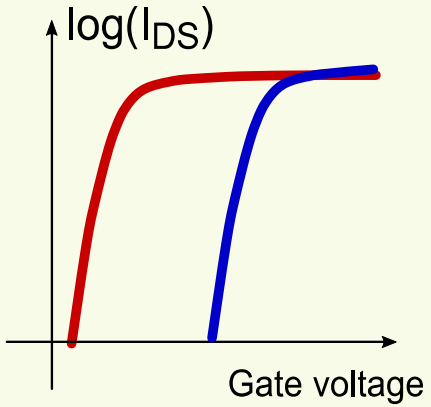
Ferroelectric displacement current



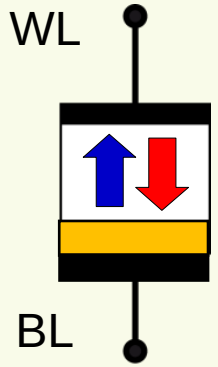
FeFET



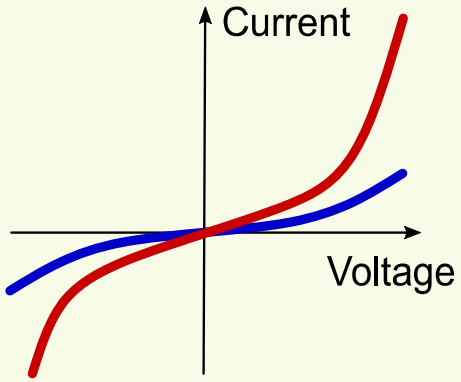
V_T shift due to polarization charges



FTJ

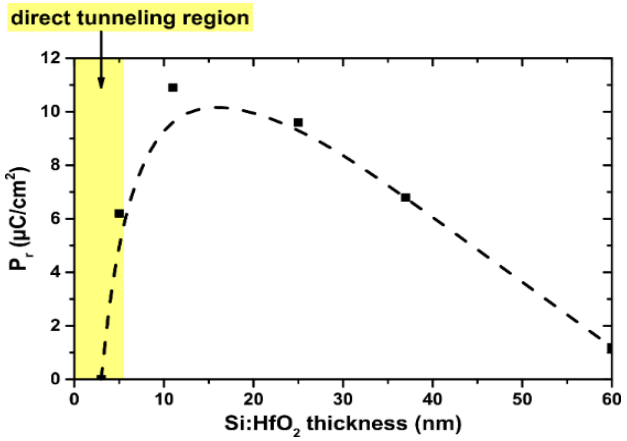


Polarization-dependent tunneling current



Funded by the European Union

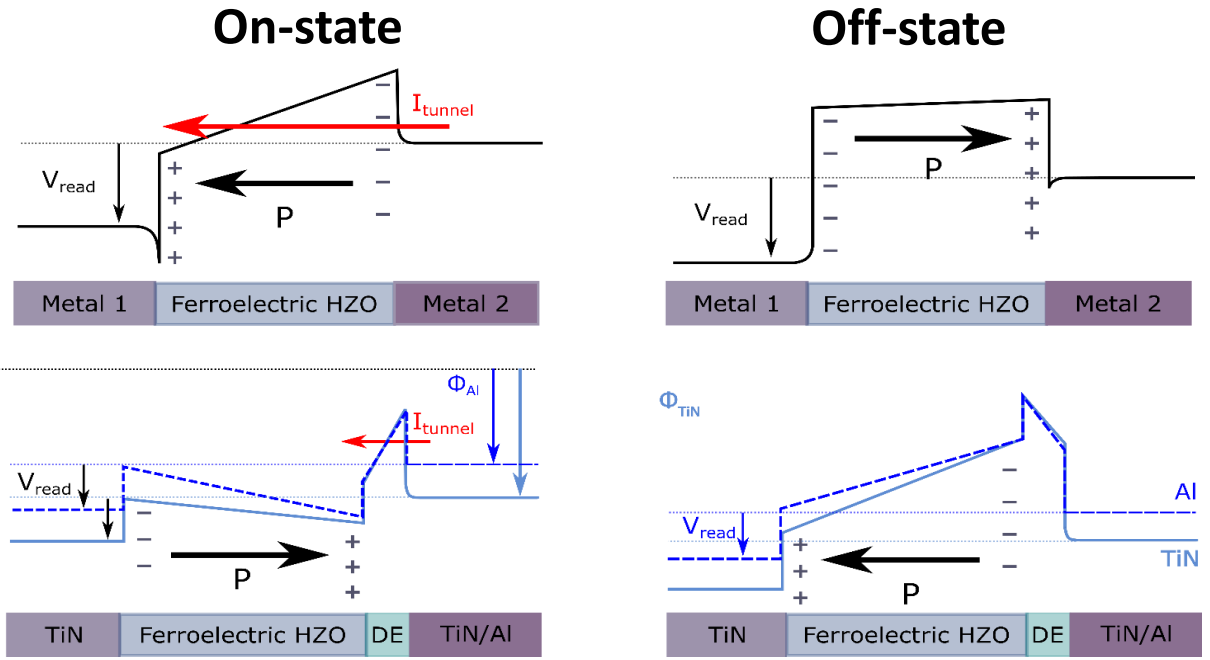
FTJ – basic principle



C. Richter et al., Adv. Electr. Mat. 3, 1700131, 2017

Single layer FTJ

Double layer FTJ



- The ferroelectric polarization alters the effective tunneling barrier
- Stable ferroelectric properties in our hafnia-based compounds only **for thickness > 5-8 nm** (down to 2nm was reported in literature)
- **Separation of switching and tunneling layer**

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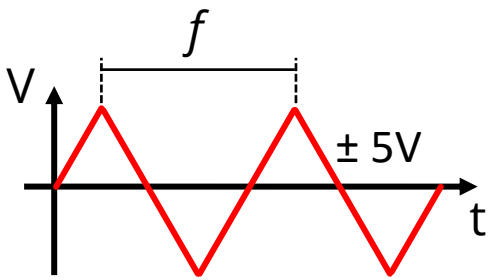
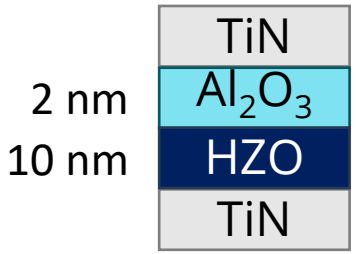
FTJ programming characteristics

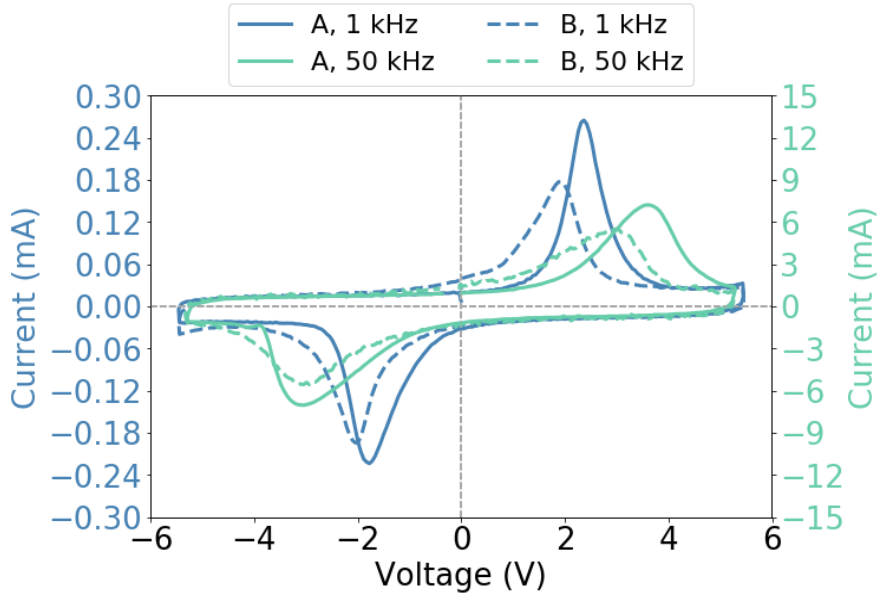
FIXIT

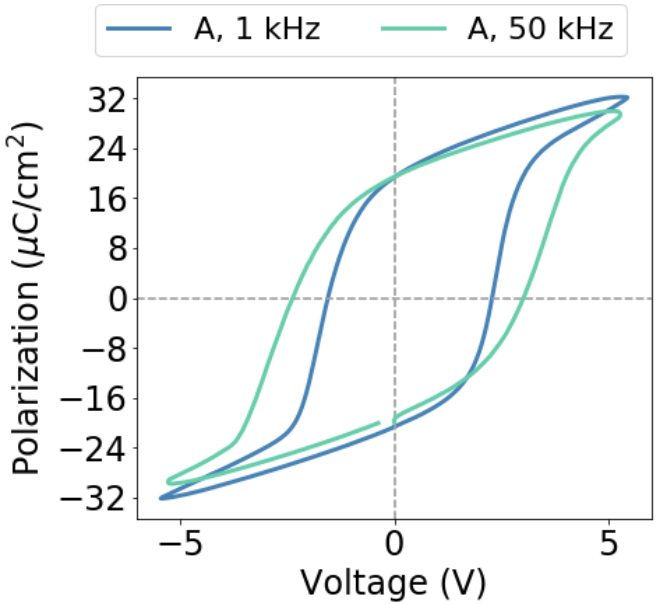




Crystallization annealing

With TiN Without TiN



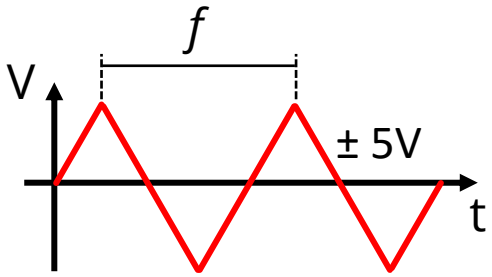


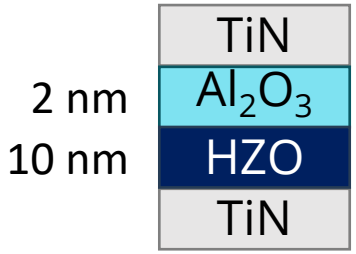
- The switching current consists of polarization and dielectric displacement current
- The switching current scales linearly with the frequency

Funded by the European Union

FTJ programming characteristics

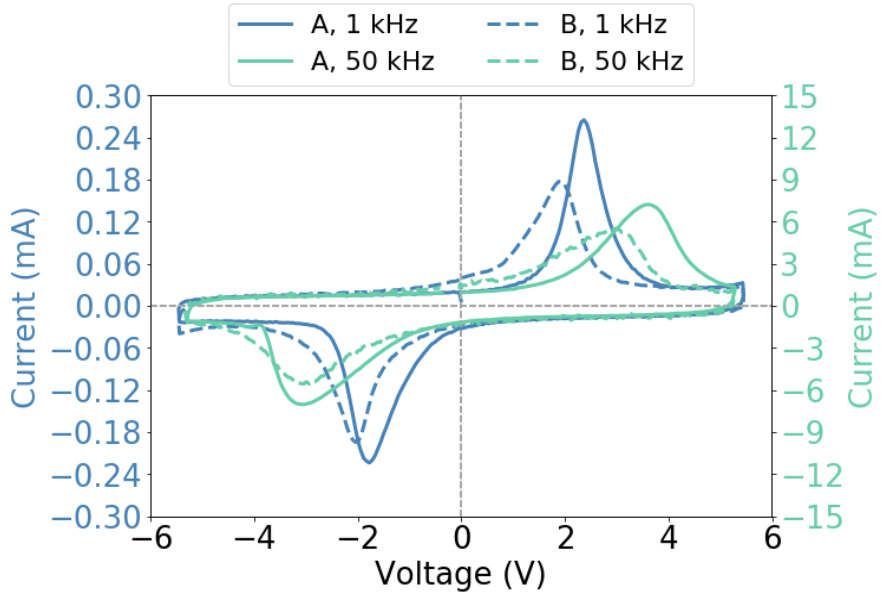
FIXIT



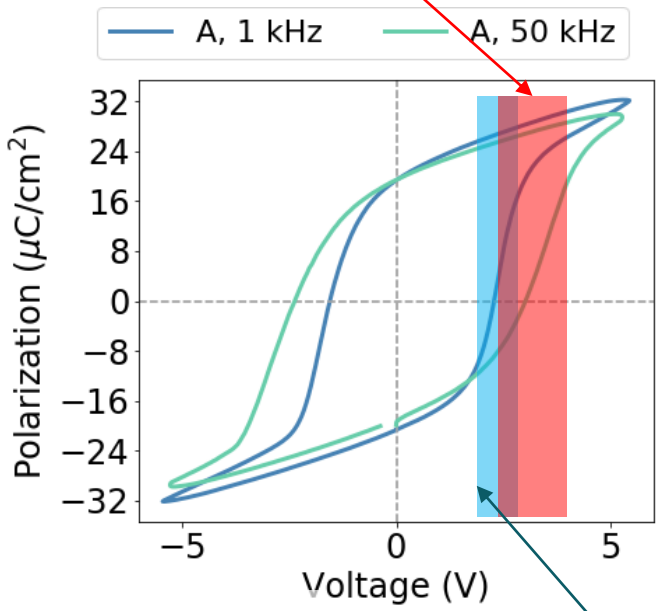


Crystallization annealing

With TiN Without TiN



Gradual switching: **analog** operations



Steep switching: **digital** operations

- The switching current consists of polarization and dielectric displacement current
- The switching current scales linearly with the frequency
- The polarization switching kinetics depend on the frequency as well
- Small changes in the material stack can have strong influence on the switching kinetics

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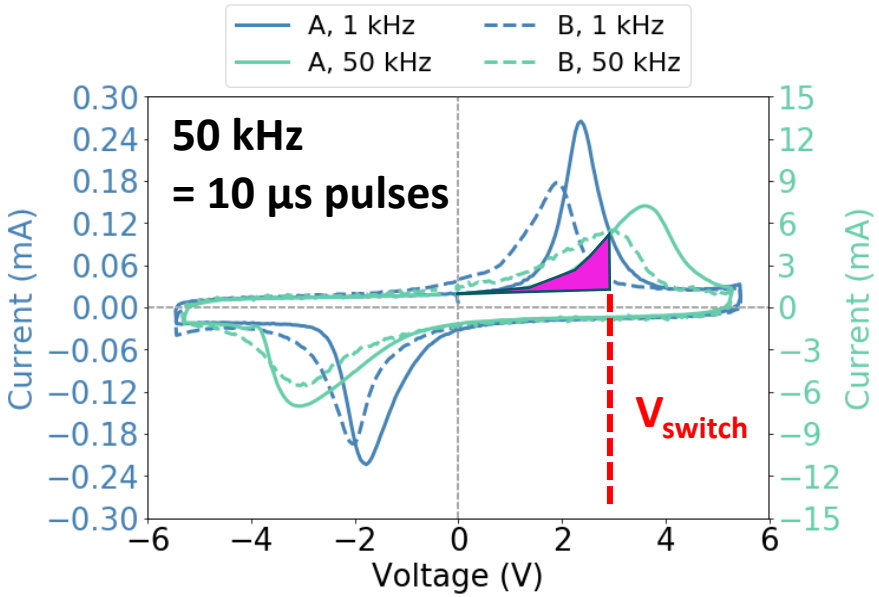
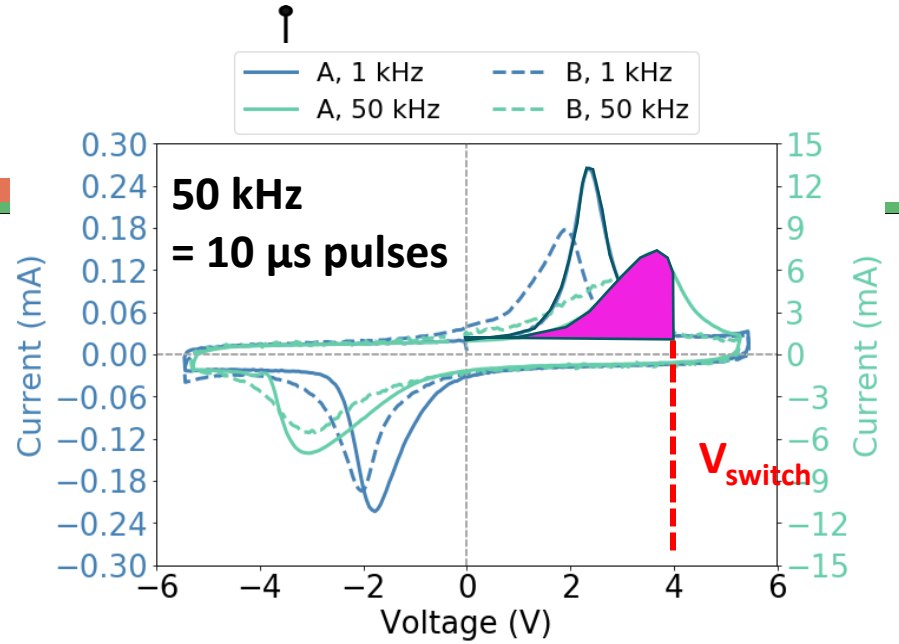
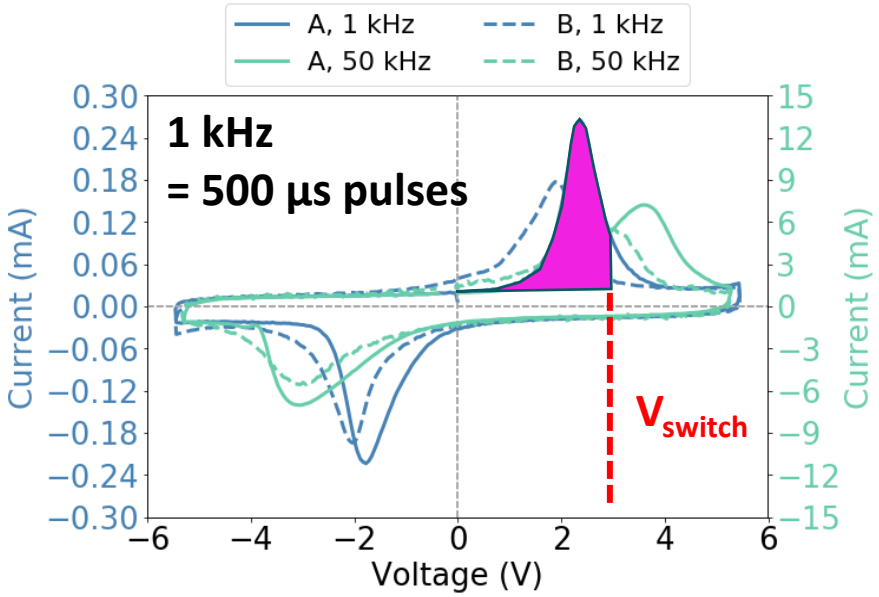
Partial weight update in FTJs



Increasing V_{switch}



Increasing t_{pls}



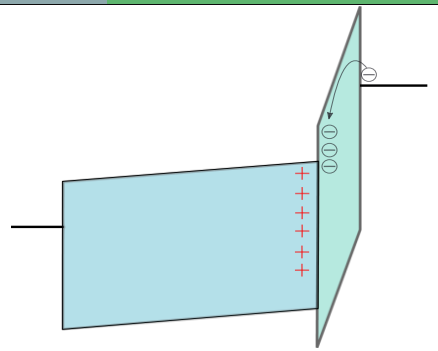
- In order to switch additional domains, amplitude/time should be increased,
- *or* we need to rely on additional device mechanism (e.g. charge accumulation)

Funded by the European Union

On-currents and switching in FTJs

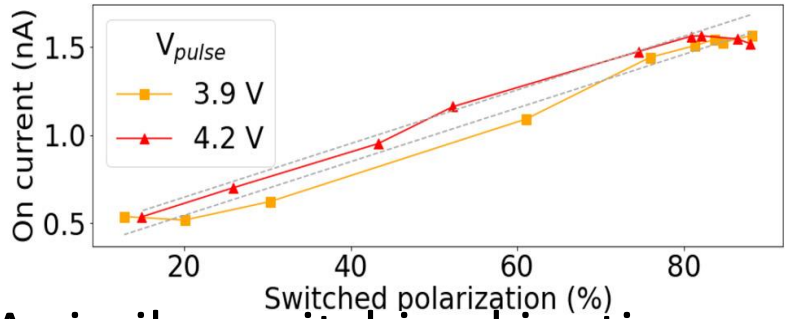
FIXIT

- Linear relation betwen on-current and area (J ~ some pA / µm²)

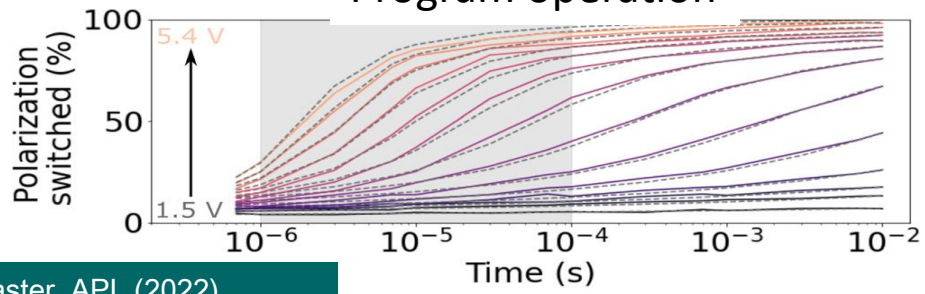


FTJ band diagram during read

- Linear relation between on-current and polarization

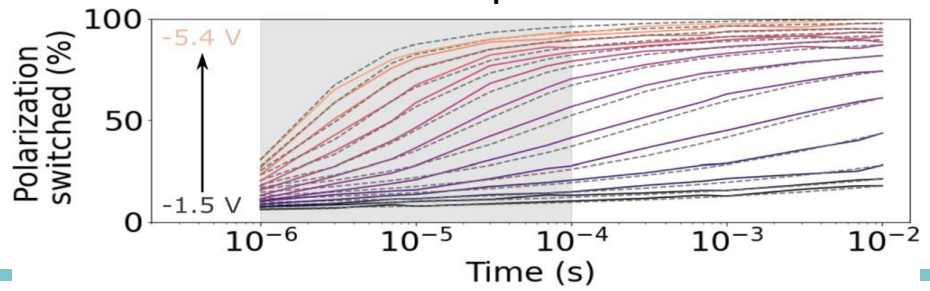


Program operation



S. Lancaster, APL (2022)

Erase operation



- A similar switching kinetic as in FeFETs can be observed

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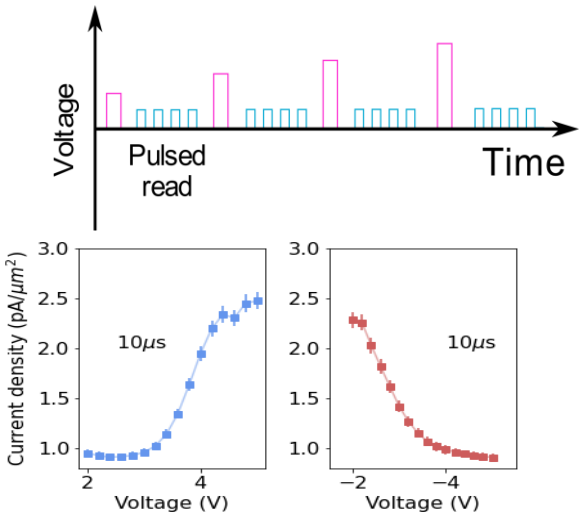
Conductance modulation

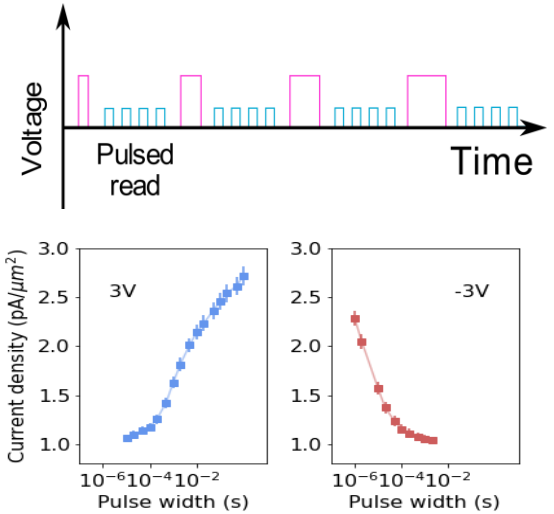
FIXIT

Voltage modulation



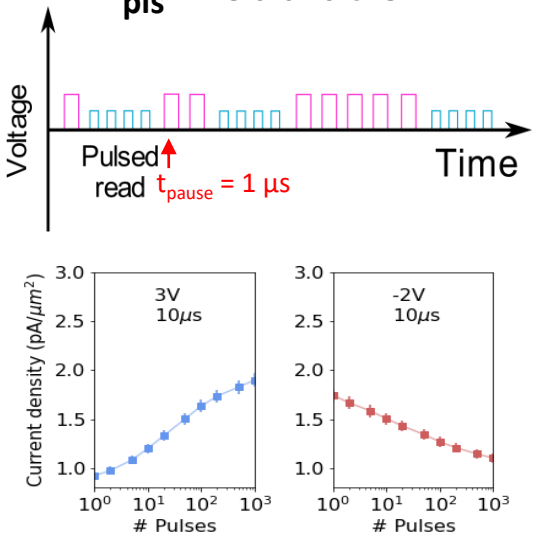
+ Largest conductance range
- Asymmetric

Time modulation



+ Pulse width easier to change on-chip than voltage
+ Medium conductance range

N_{pls} modulation



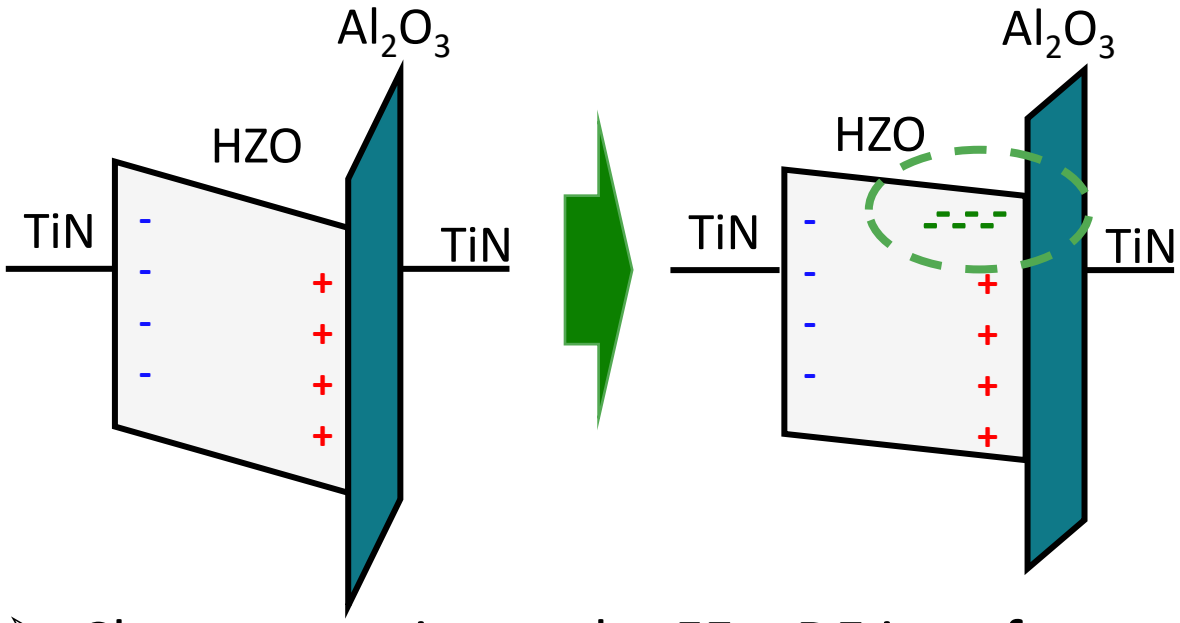
+ Easiest on-chip application
- Small conductance range
- Known (small) wait time between pulses necessary

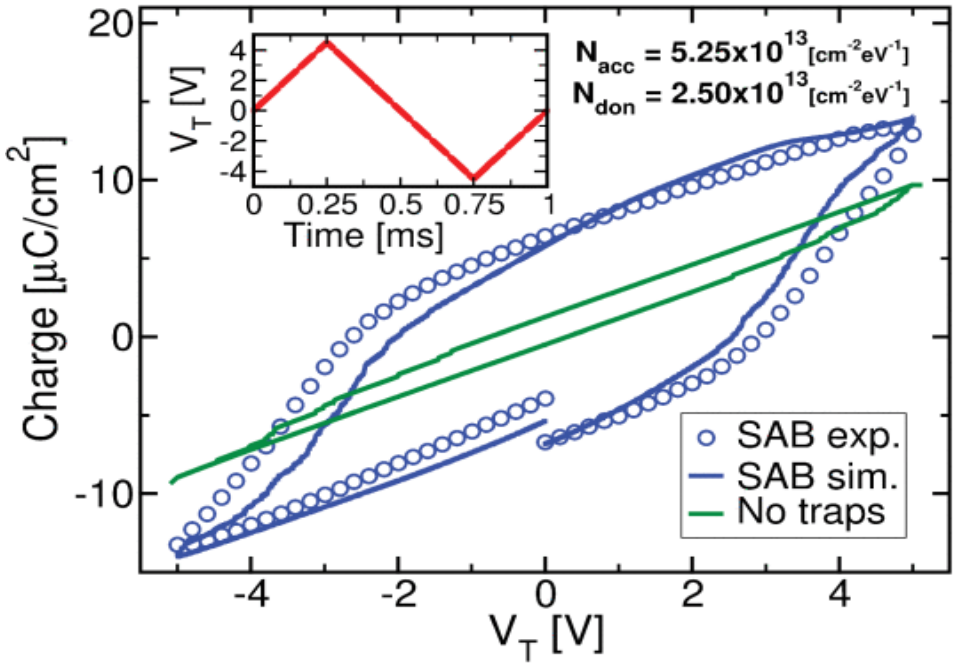
➢ **The programming algorithm affects the weight update → DTCO**

Funded by the European Union

The impact of charge trapping on switching

FIXIT





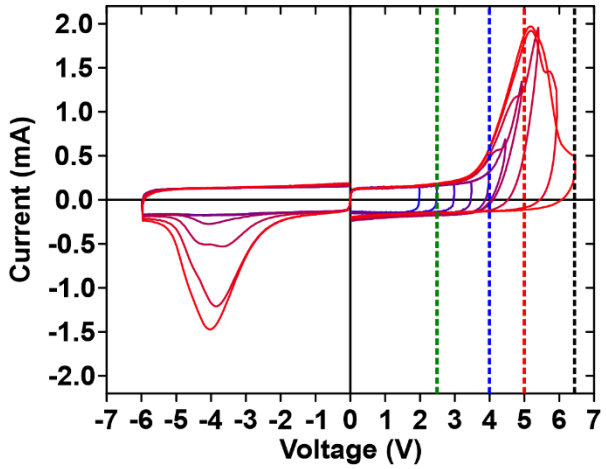
R. Fontanini et al., TED vol. 69, no. 7, pp. 3694-3699, 2022.

- Charge trapping at the FE – DE interface
  - increases switching field and
  - decreases the depolarizaiton field
- **Charge trapping is mandatory for double-layer FTJ operation**
- **Trapped electrons can lower the read current !!**

Funded by the European Union

Transient current vs. DC-current

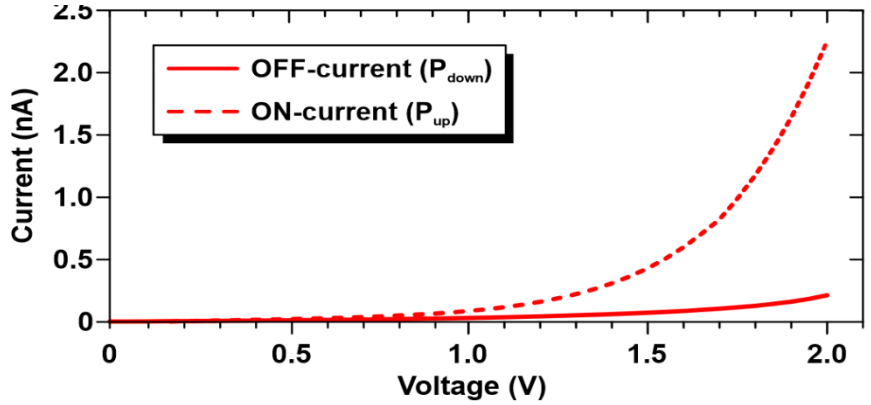
FIXIT



IV-response during polarization switchign

200µm FTJ measurements

100uA vs. 1nA



IV-response during DC read operation

- Polarization switching currents can be much larger than the DC-currents
- During read operation any transient switching has to be omitted

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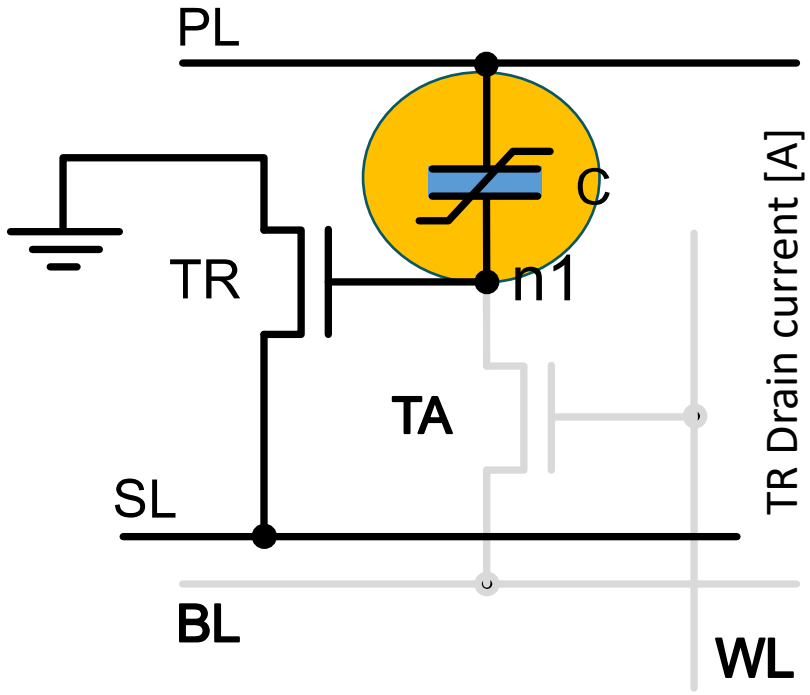
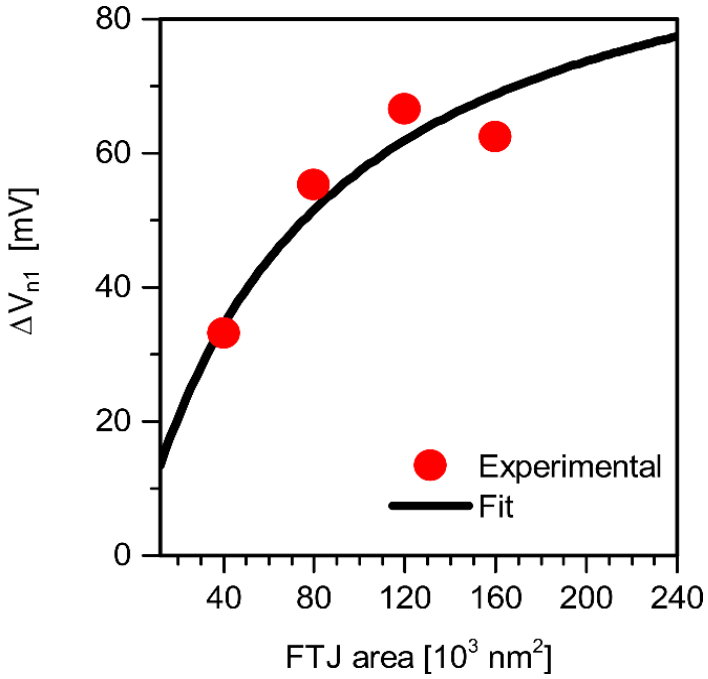
FTJ area and self capacitance



$$\Delta V_{n1} = \frac{A_{FTJ} \cdot J_{FTJ} \cdot time}{(C_{gate} + C_{FTJ})}$$



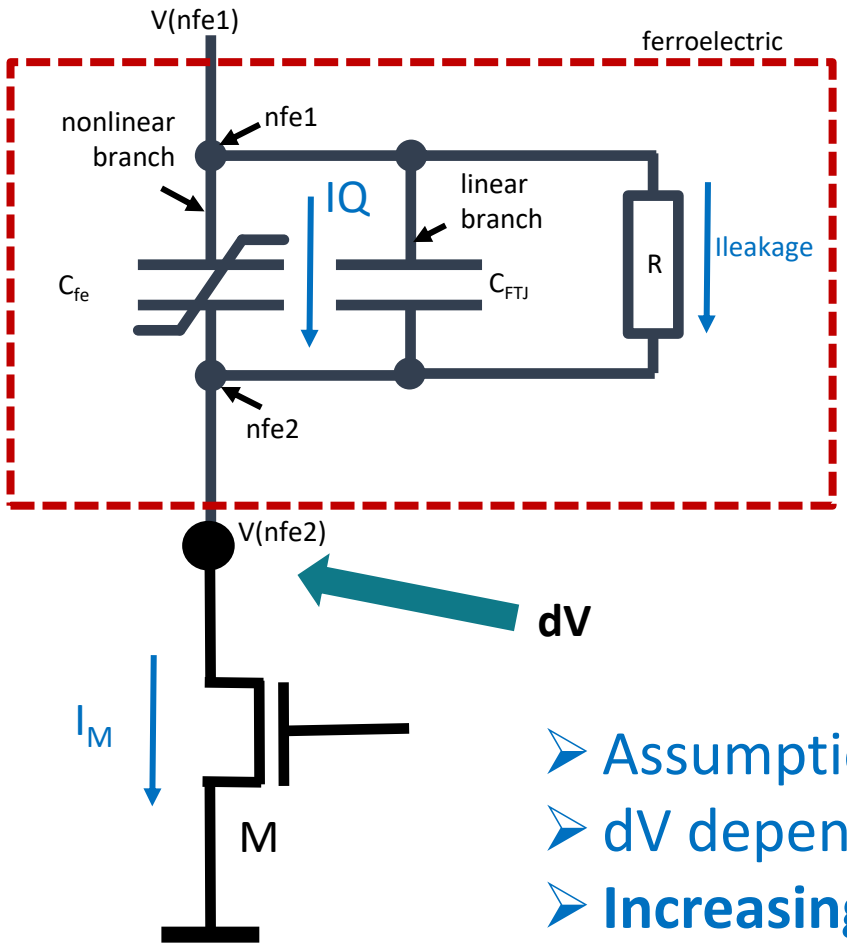
- Signal development at n1 after 100µs **~ some 10mV**
- Increasing FTJ area and time increases the signal
- For large FTJ: self-capacitance of FTJ limits the signal

S. Slesazeck et al., IMW, 2019

Funded by the European Union

FTJ area scaling – impact on signal development

FIXIT



C_{FTJ} = **16fF / um²**

I_{on} = 10pA/um²

I_{off} = 1.5pA/um²

Calculate dV in readout case: C = I * t / dV

dV_{on} = I * t / C = 10pA * 100us / 16fF = 62mV

dV_{off} = I * t / C = 1pA * 100us / 16fF = 6 mV

$dV = dV_{on} - dV_{off}$ = 56mV after 100us

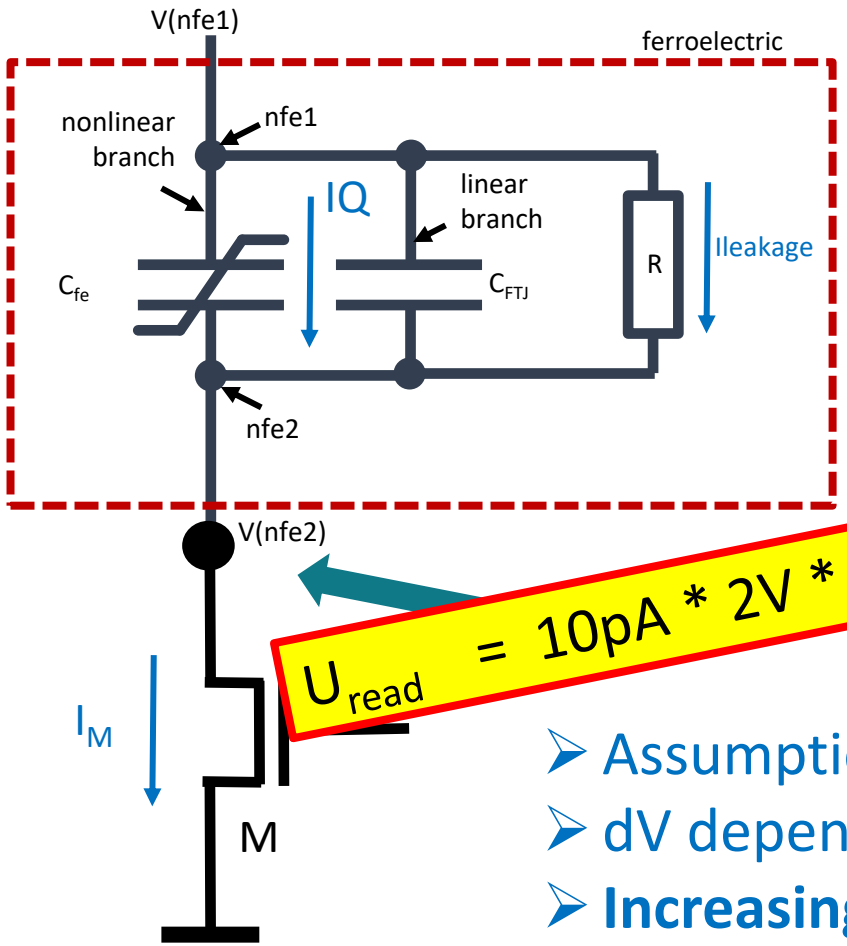
$$dV = \frac{I * t}{C_{FTJ}} = \frac{n * I * t}{n * C_{FTJ}}$$

- Assumption: $C_{FTJ} >> C_M$
- dV depends mainly on I_{on} and I_{off} and C_{FTJ}
- **Increasing FTJ area does not increase the dV!**
- **Readout is slow → parallel operation!**

Funded by the European Union

FTJ area scaling – impact on signal development

FIXIT



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dV_{off} = I * t / C = 1pA * 100us / 16fF = 6 mV

U_{read} = 10pA * 2V * 100us = 2 fJ

$_{off}$ – 56mV after 100us

$$dV = \frac{I * t}{C_{FTJ}} = \frac{n * I * t}{n * C_{FTJ}}$$

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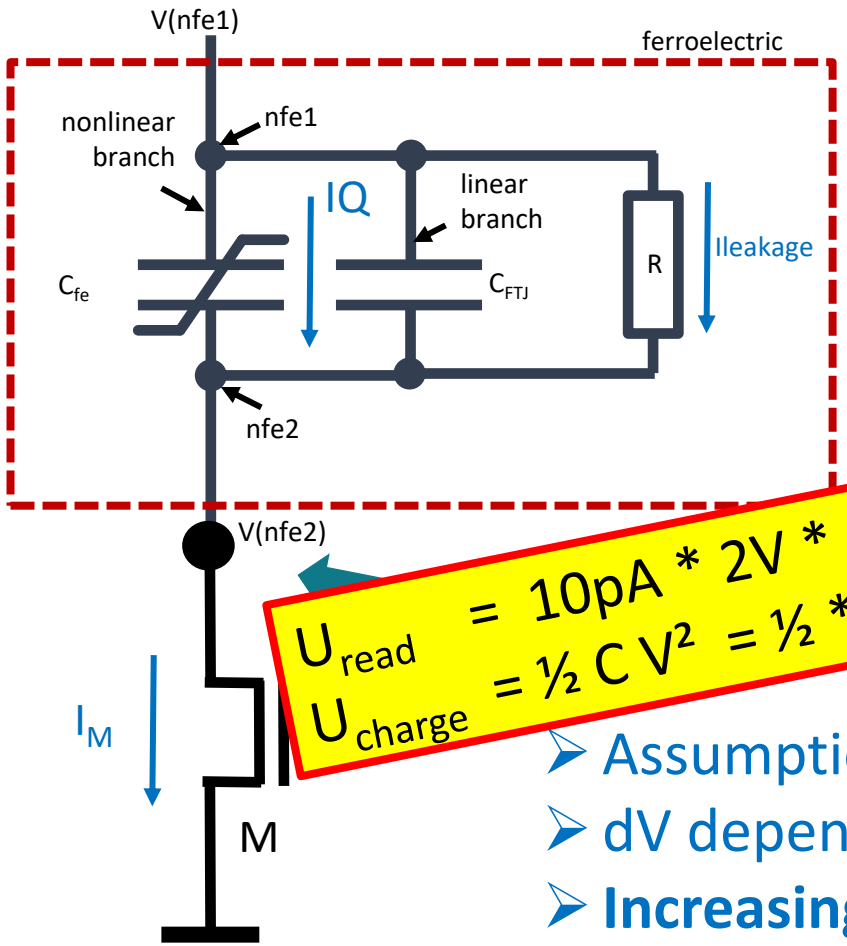
Funded by the European Union

FTJ area scaling – impact on signal development

FIXIT



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dV_{off} = I * t / C = 00us / 16fF = 6 mV

after 100us

U_{read} = 10pA * 2V * 100us = 2 fJ

U_{charge} = ½ C V² = ½ * 16fF * 2V² = 32 fJ

$$dV = \frac{I * t}{C_{FTJ}} = \frac{n * I * t}{n * C_{FTJ}}$$

- Assumption: $C_{FTJ} >> C_M$
- dV depends mainly on I_{on} and I_{off} and C_{FTJ}
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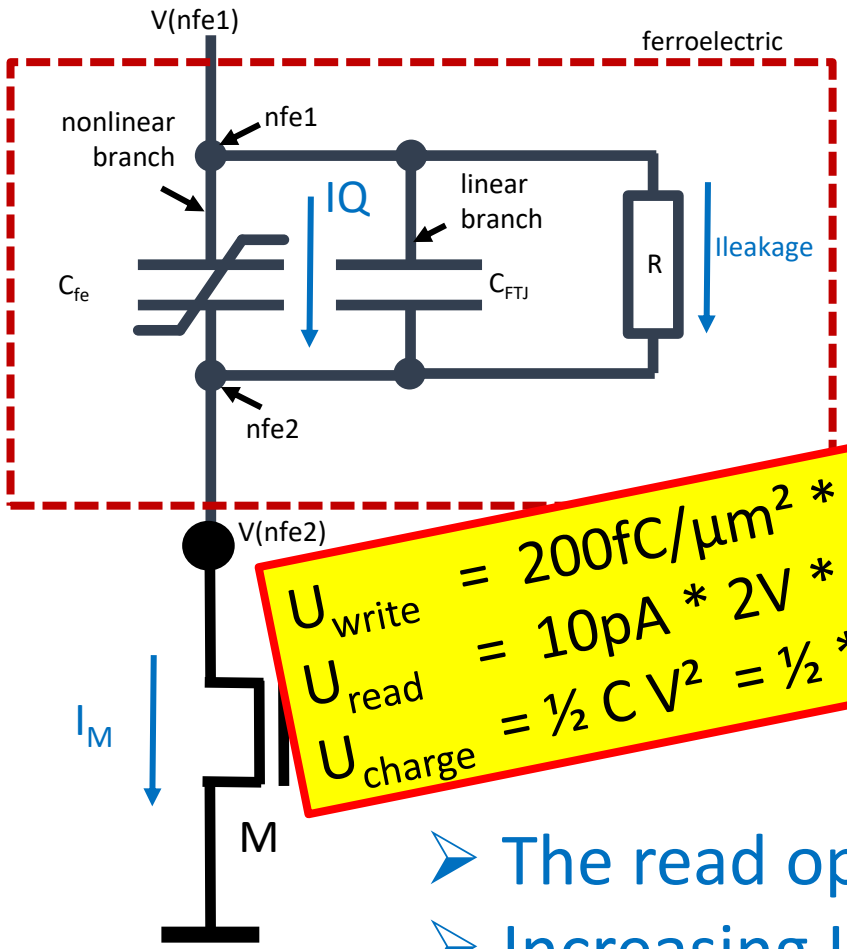
FTJ area scaling – impact on signal development

FIXIT



C_{FTJ} = **16fF / um²**

I_{on} = 10pA/um²

I_{off} = 1.5pA/um²

Calculate dV in readout case: C = I * t / dV

dV_{on} = I * t / C = 100us / 16fF = 62mV

= 00us / 16fF = 6 mV

after 100us

U_{write} = 200fC/µm² * 4V = 800fJ

U_{read} = 10pA * 2V * 100us = 2 fJ

U_{charge} = ½ C V² = ½ * 16fF * 2V² = 32 fJ

$$dV = \frac{I * t}{C_{FTJ}} = \frac{n * I * t}{n * C_{FTJ}}$$

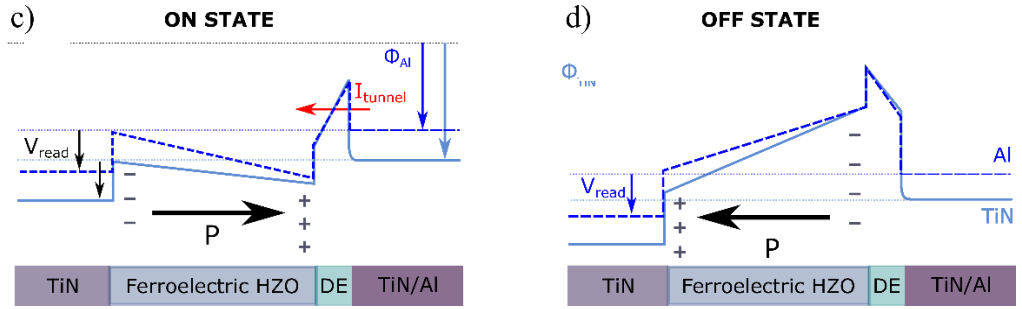
- The read operation is very energy efficient – 2fJ / µm²!
- Increasing I_{on} could lower the write energy.

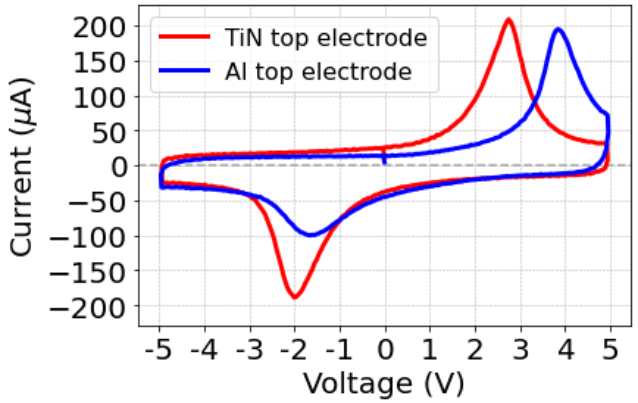
Funded by the European Union

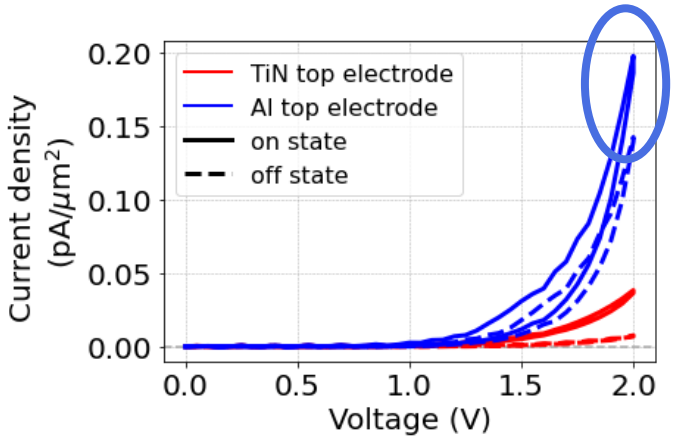
Improving FTJ current densities

Work function engineering: lower Φ

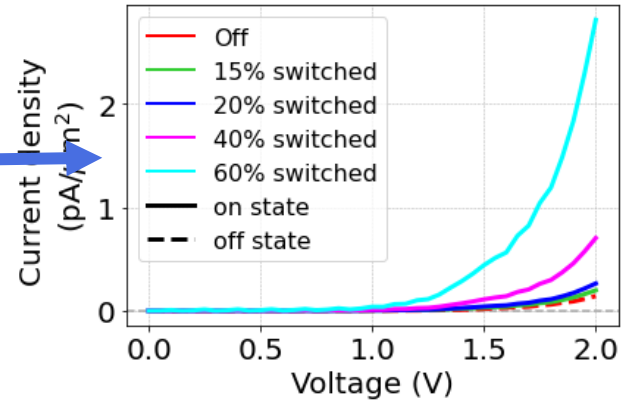
- TiN (4.7 – 5.2 eV) → Al (4.0 – 4.2 eV)
- I_{on} and I_{off} increase







Estimated only ~20% domains contribute to ‚On'-state (high P_{loss})



- **Improved current density, but imprint = fast loss of I_{on}**
  - **Poor retention due to large built-in field**
- **Oxidation of electrode over time**

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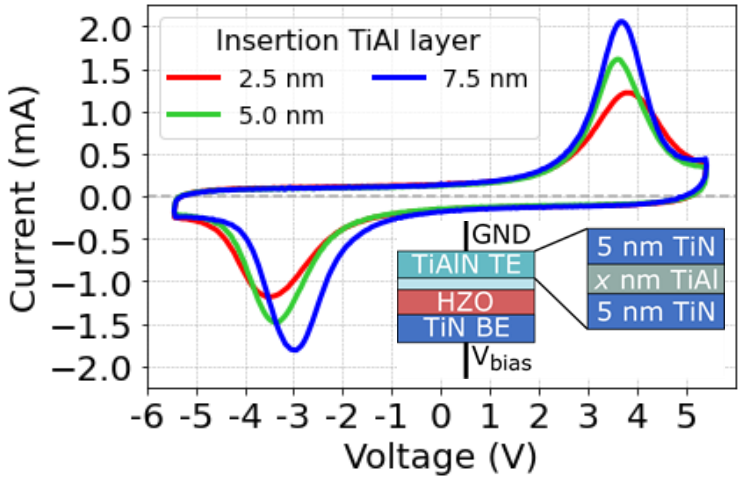
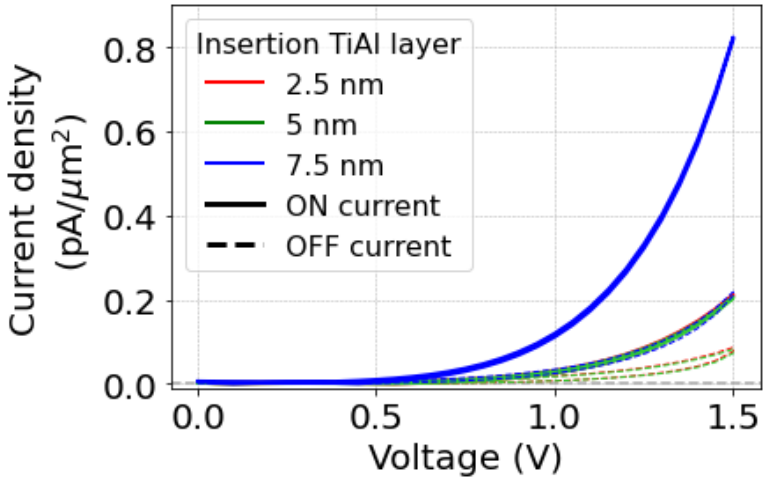
Improving FTJ current densities





- Doping Al into TiN electrodes reduces work function:
  - Maintain chemical stability of electrode-FE interface
  - Switching remains symmetrical
  - BEOL-compatible process

S. Lancaster, ESSDERC 2022, Milan, Italy

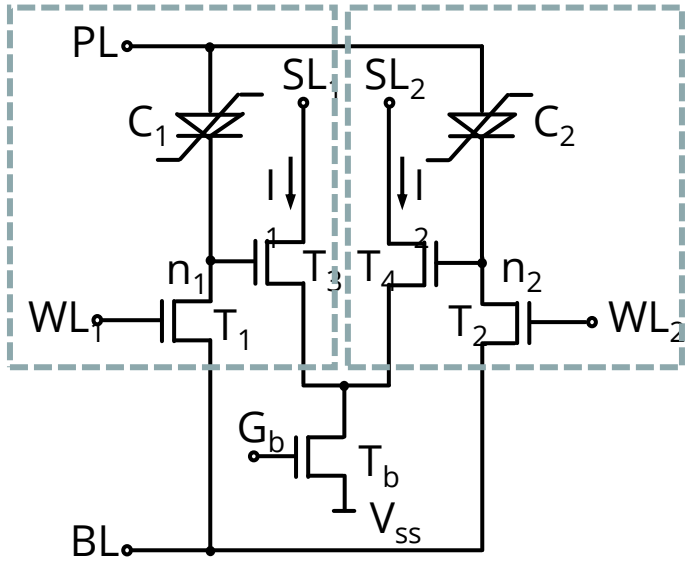
- Tunneling current (→ WF) controllable by thickness of TiAl insert
- **I_{on} improvement more than 10x**

Funded by the European Union

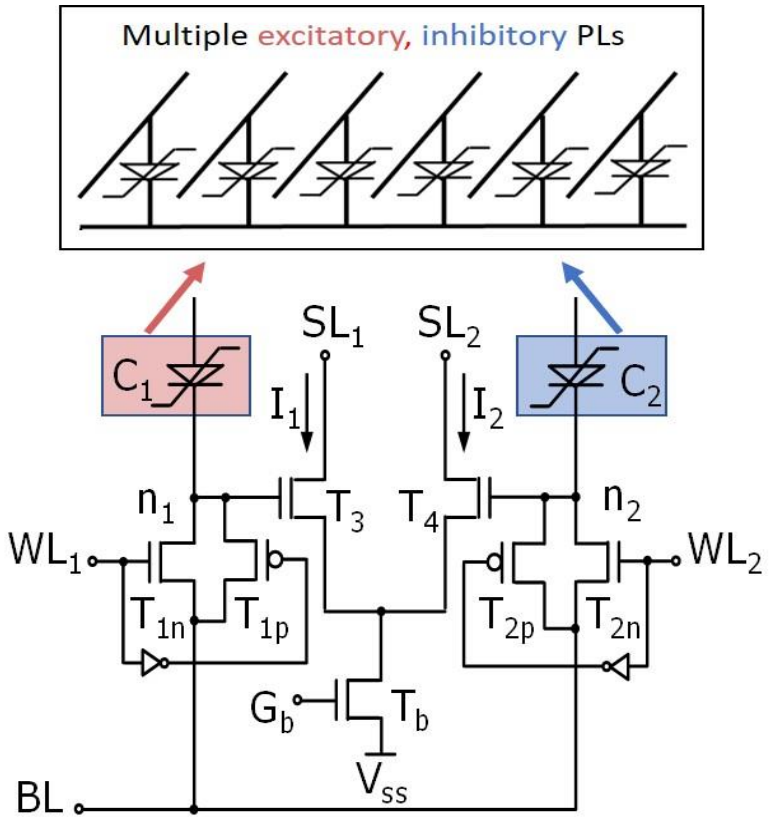
Parallel FTJ operation

Differential synaptic cell

- Connect many FTJs in parallel at C_1 and C_2,
- Each FTJ can act as a single weighting element e.g. for analog operation, but
- Readout of single FTJs is precluded



Covi et al., ISCAS 2021

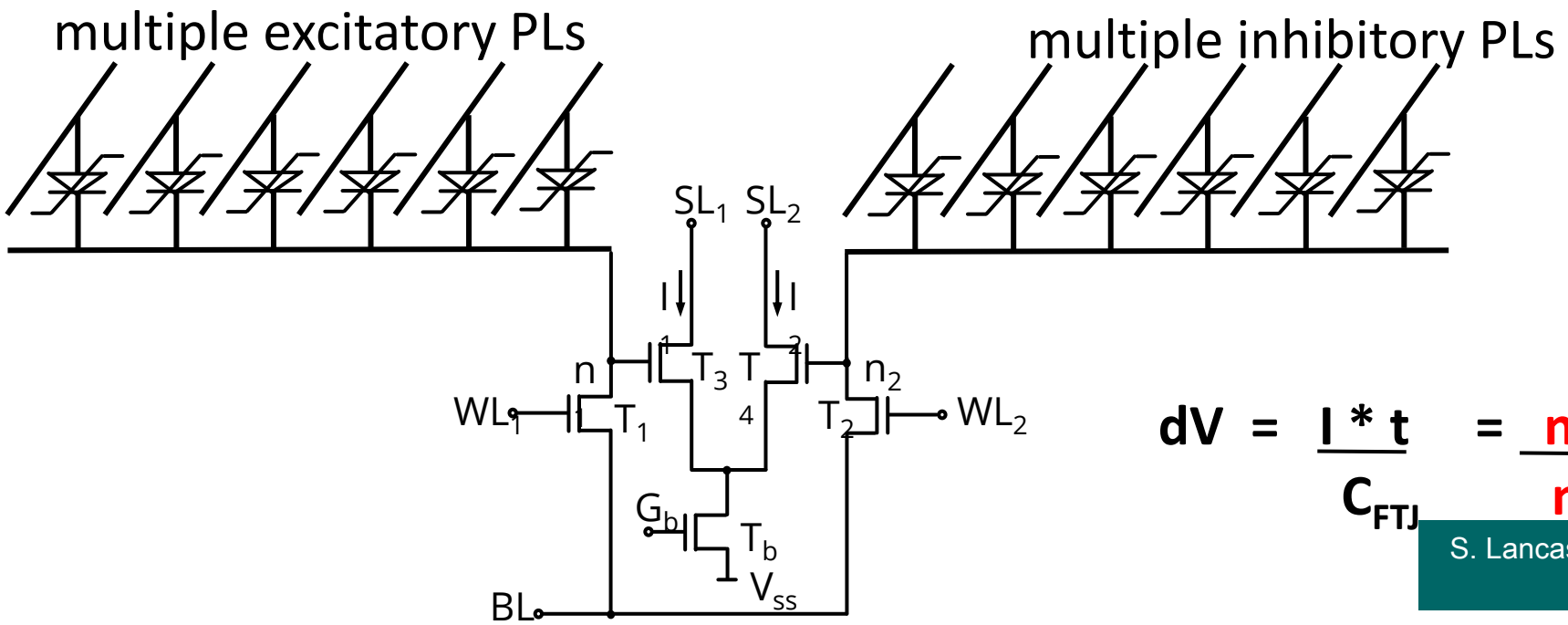


- **Less circuit overhead when using multiple FTJs for one read circuit**
  - ➔ **IMC, CIM, LIM, etc….**

Funded by the European Union

FTJ-based MVM in cross-bar arrays

FIXIT



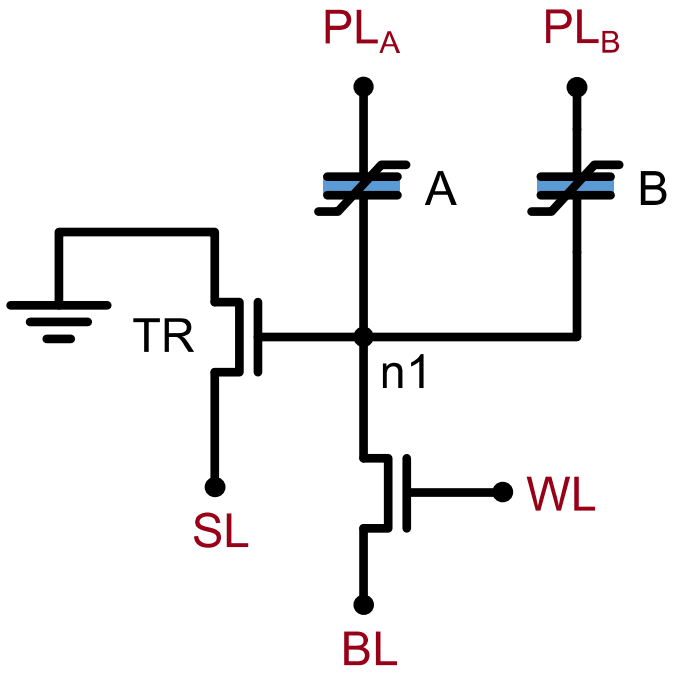
$$dV = \frac{I * t}{C_{FTJ}} = \frac{n * I * t}{n * C_{FTJ}}$$

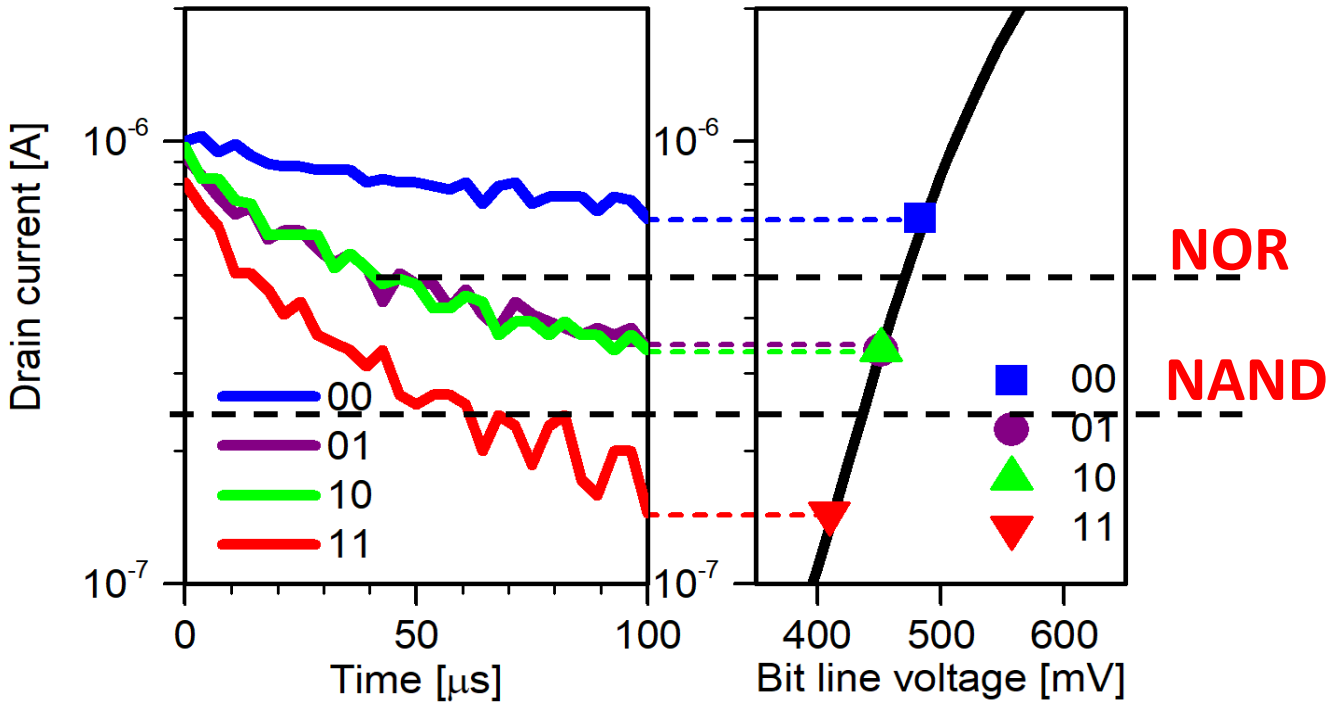
S. Lancaster, ESSDERC 2022

- Increasing the number of FTJs does not change dV_{min} and dV_{max}!
- Incfreasing J_{on} by device engineering is decisive
- The ratio of J_{on} / C_{FTJ} defines a window function, that could be interpreted as **Sigmoid or RELU** activation function …. ☺

Funded by the European Union

Multiple FTJs …





S. Slesazeck, et.al., IEDM 2019

- Application of multiple parallel FTJs reduces circuit overhead
- Example: NAND/NOR logic gate, depending on the current threshold

Funded by the European Union

Switching kinetics and read disturb

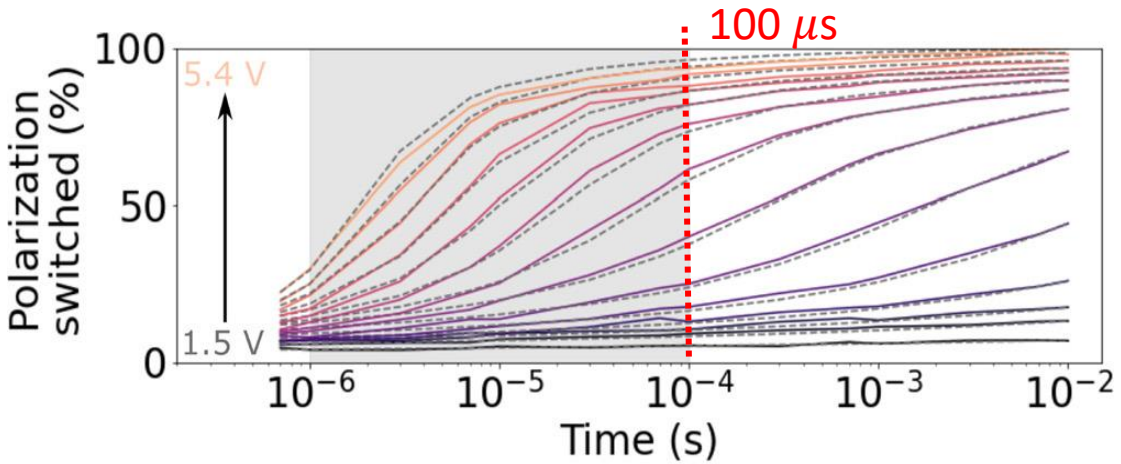
FIXIT

Assuming a polarization of **20 μC / cm²** : 200 fC / μm²
Assuming a **0,1 % polarization loss**: 0,2 fC / μm²

$dV_{on} = dQ_P / C_{FTJ}$ = 0,2 fC / 16 fF

= **12,5mV** ⇔ **dV = 56mV from Ion**

Switching kinetics measurements



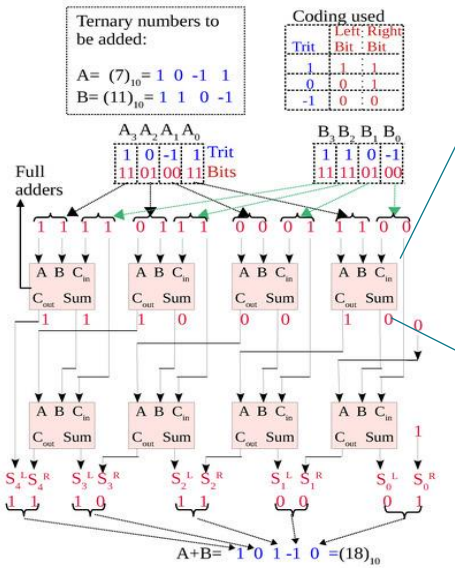
S. Lancaster, APL (2022)

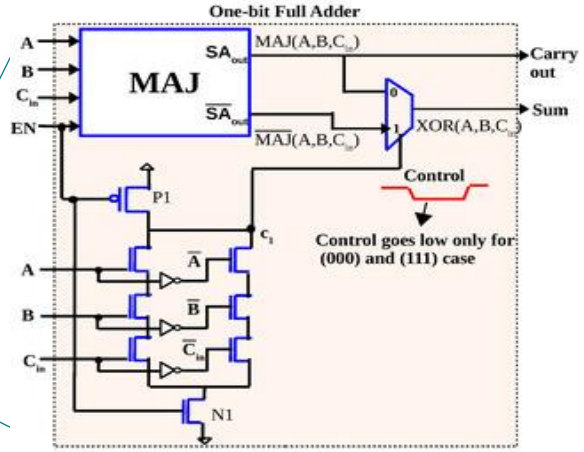
- During read operation any polarization switching has to be omitted
- There is a **tradeoff between I_{on} and polarization loss dQ_P**
- Careful device design and selection of read voltage
  → **thorough DTCO**

Funded by the European Union

Ternary Adder and Majority Operation

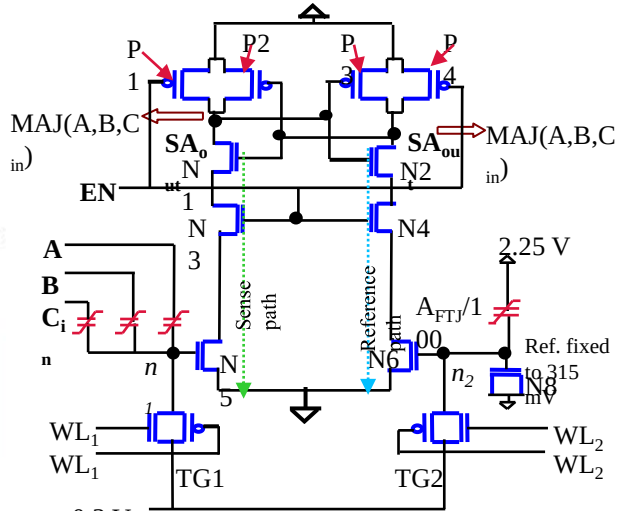
FIXIT





XOR= $\overline{MAJ}$ except for (000),(111) case

(A,B, C_{in}) Input	Carry out MAJ	Sum XOR
(000)	0	0
(001)	0	1
(010)	0	1
(011)	1	0
(100)	0	1
(101)	1	0
(110)	1	0
(111)	1	1



NVM Device	Energy	Latency	Power	Ref.
ASL-PMA	3.68 pJ	29 ns	0.12 mW	[32]
STT-MRAM	4.2 pJ	0.6 ns	7 mW	[33]
SOT-DW	0.031 pJ	495 ns	62.6 nW	[7]
FTJ	**0.78 pJ**	**100 µs**	**7.8 nW**	**This work**
CMOS	0.1 pJ	0.4 ns	0.25 mW	[7]

- Computing with three states enables “carry-free addition”
- Majority gate is a basic building block for ternary addition
- Ultra-low power ternary adder using FTJ for addition of very large vectors

→ **decreasing latency**

Reuben, John, et al. Electronics 12.5 (2023): 1163.

Funded by the European Union

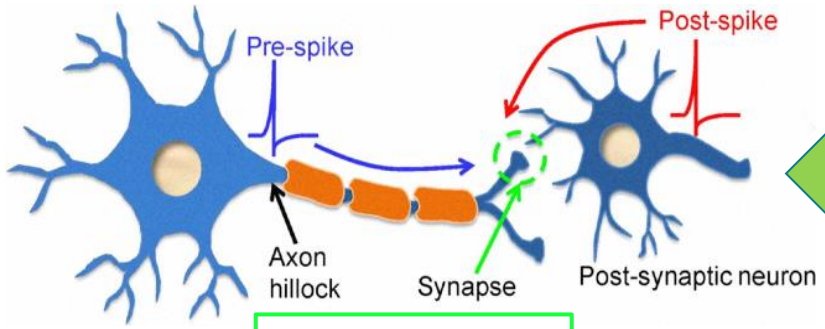
- Introduction
- Ferroelectric memory devices
  - Ferroelectric capacitor - FeCAP (for FeRAM)
  - Ferroelectric Field Effect Transistor - FeFET
  - Ferroelectric Tunneling Junction - FTJ
- **Ferroelectrics for unconventional computing**
- Ferroelectric device comparison
- Conclusion

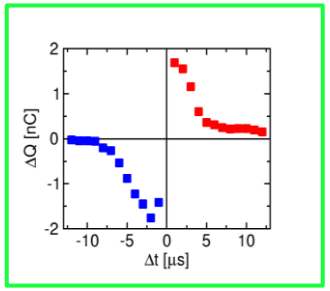
Funded by the European Union

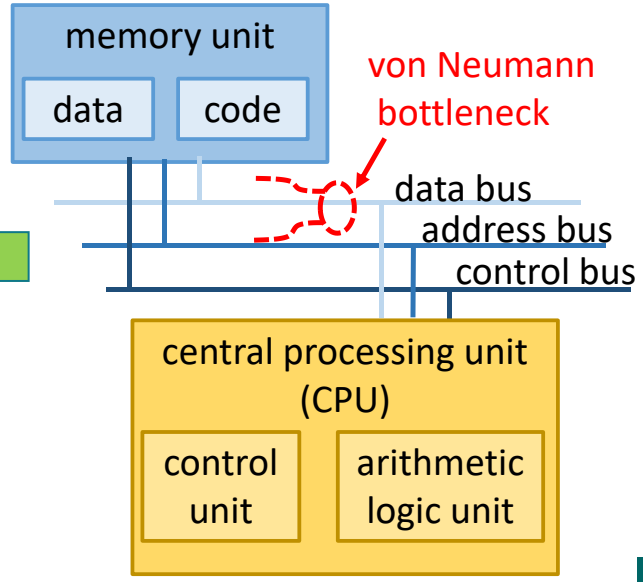
Increasing computing complexity for big data

and AI demand for **new computing architectures**

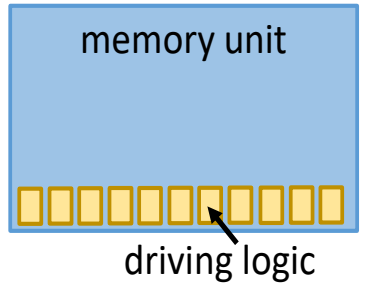
Neuromorphic Computing



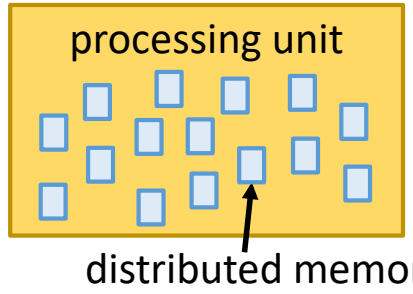




Compute in Memory



Logic in Memory



S. Slesazeck, T. Mikolajick, Nanotechnology (2019)

➢ Memory remains one of the most important ingredients of electronic devices

Funded by the European Union

Societal and Technologigal evolution → AI ⟷ **Climate change**

- Worst case scenarios 2030: 1/3 of world-wide energy is eaten up by IT

ChatGPT's Electricity Consumption

ChatGPT may have consumed as much electricity as 175,000 people in January 2023.

https://towardsdatascience.com/the-carbon-footprint-of-chatgpt-66932314627d 25th of April 2023

- **A new energy-aware IT needs**
  - **low-power technologies**
  - **new computing concepts combining logic and memory functionality**

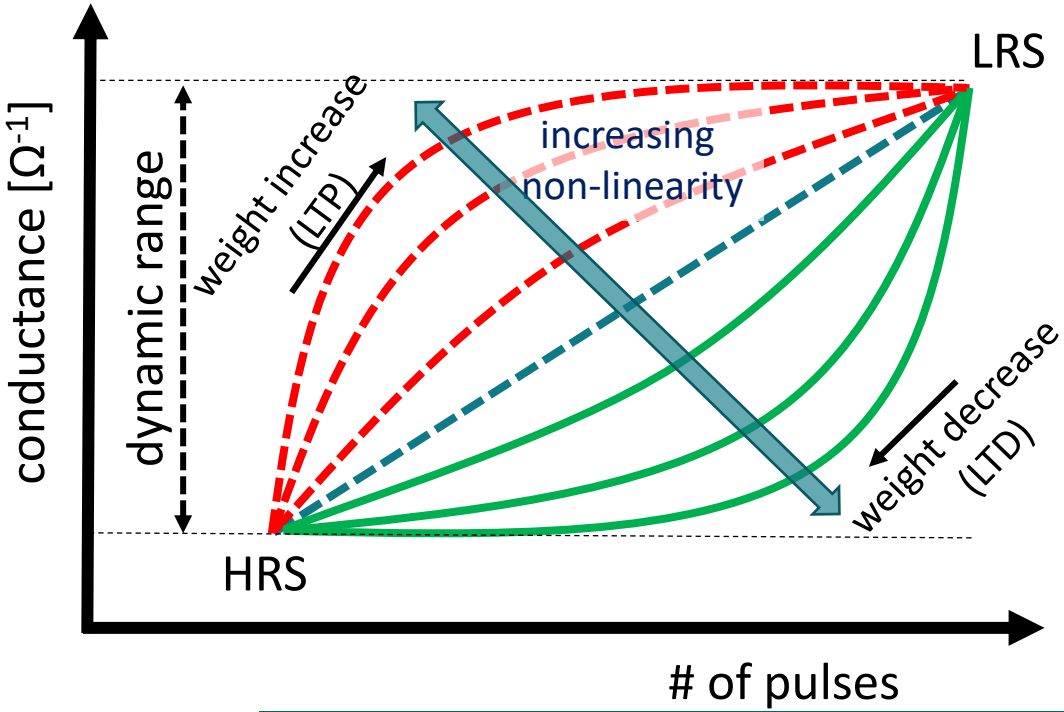
Funded by the European Union

General:

Highly parallel operation	→ high impedance devices
	→ scalability
Energy efficiency	→ low voltage operation
	→ low write currents
	→ non-volatility
On-line learning	→ cycling endurance

Spiking Neural Networks:

Linearity	→ switching kinetics
Symmetry	→ switching kinetics
Dynamic range	→ multi-level, variability



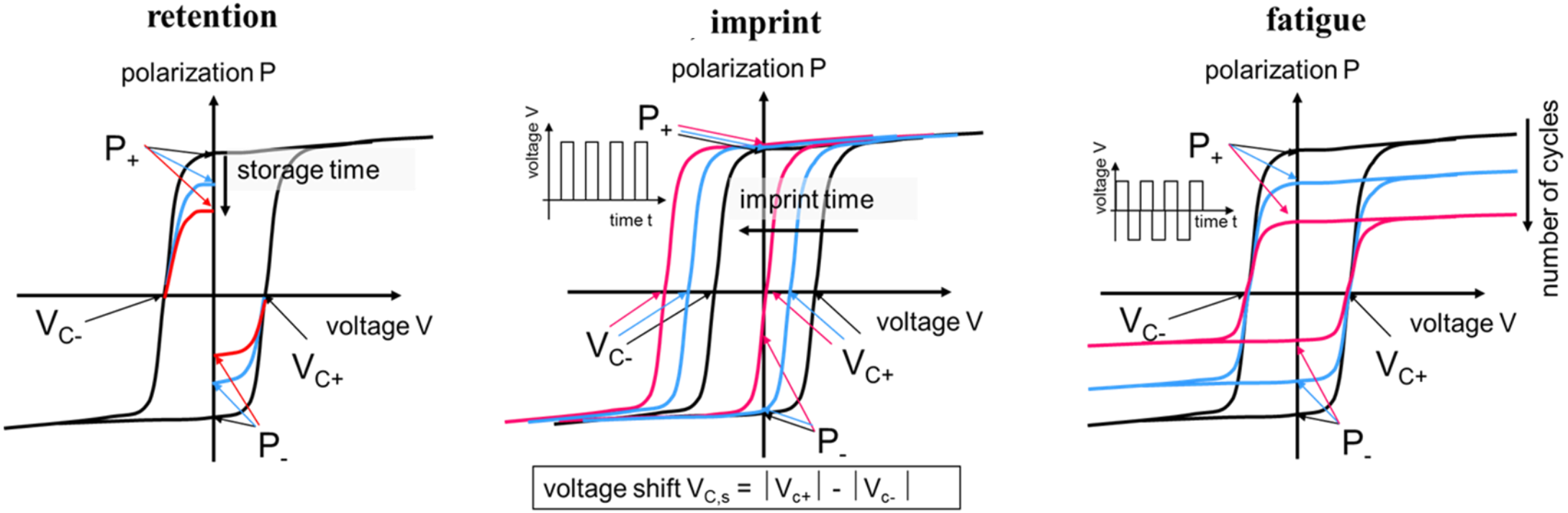
S. Slesazeck, T. Mikolajick, Nanotechnology (2019)

➢ Application dependent device requirements
beyond the needs of conventional memory

Funded by the European Union

Reliability Aspects of Ferroelectric Materials

FIXIT

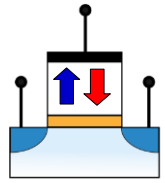


- Retention: Depolarization as a function of time
- Imprint: Parallel shift of hysteresis as a function of time
- Wake-up: Increase of polarization with field cycling in the early phase
- Fatigue: Loss of polarization with field cycling

T. Mikolajick, Ref. Mod. in Mat. Sc. and Mat. Eng., Elsevier 2016

Funded by the European Union

Single Domain switching kinetics

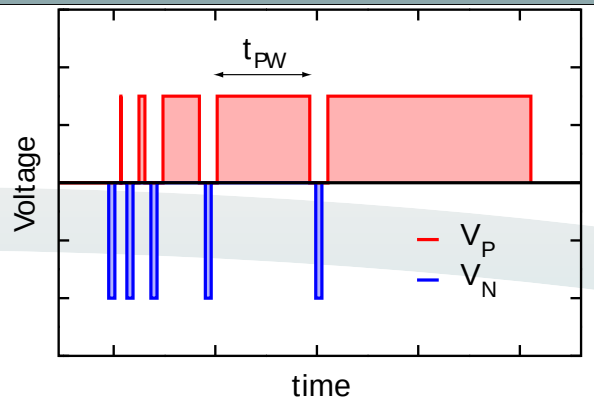


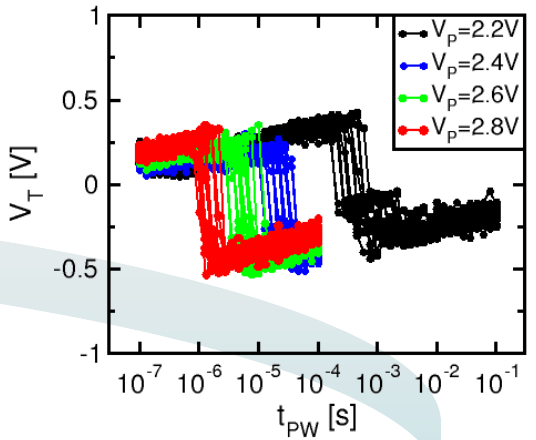
FIXIT

Ultra-scaled FeFETs:

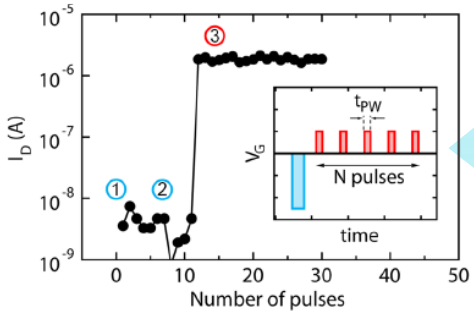
- *W*=80 nm
- *L*=30 nm

TEM
top-view

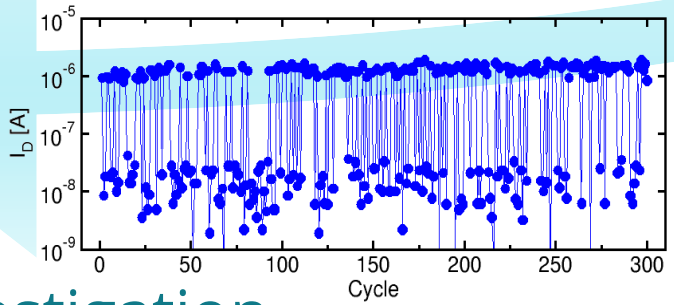


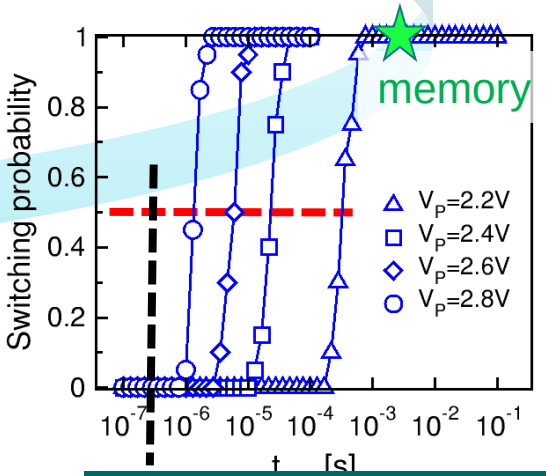


accumulative switching - neuron



random number generation





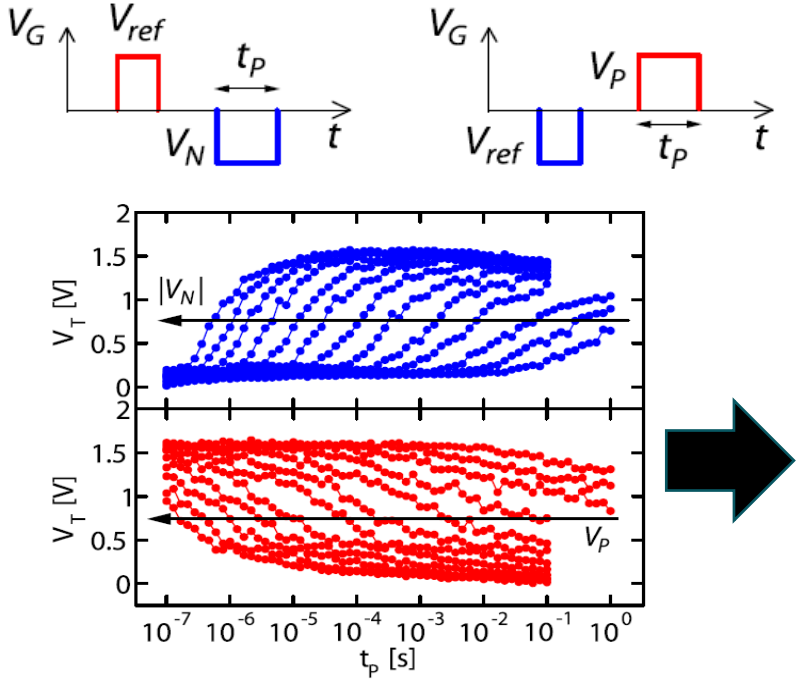
➢ Small FeFETs allow the investigation of single domain switching

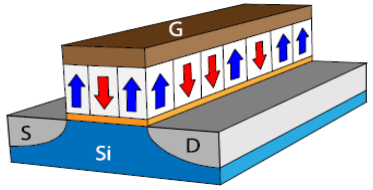
H. Mulaosmanovic et al., IEDM, (2015)
H. Mulaosmanovic et al., VLSI, (2017)
H. Mulaosmanovic et al., Nanoscale, (2018)

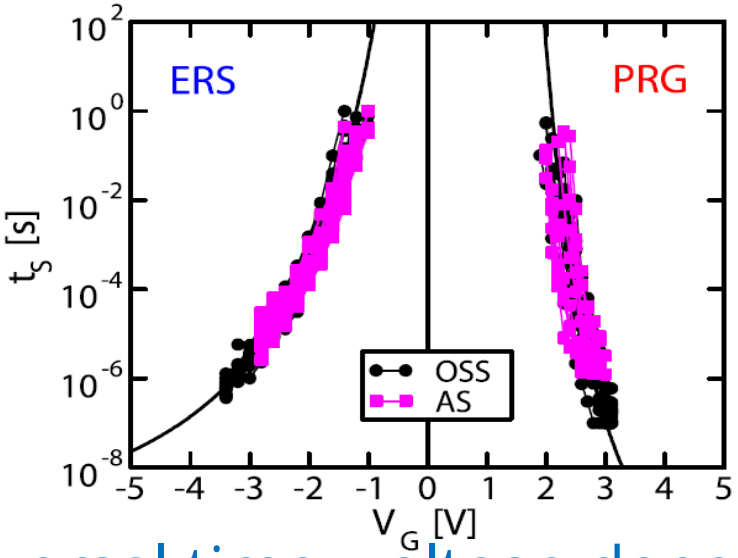
Funded by the European Union

Gradual switching in FeFETs - Linearity

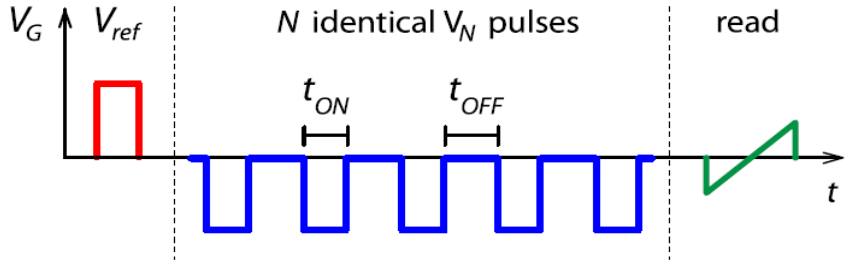
One Shot Switching (OSS)

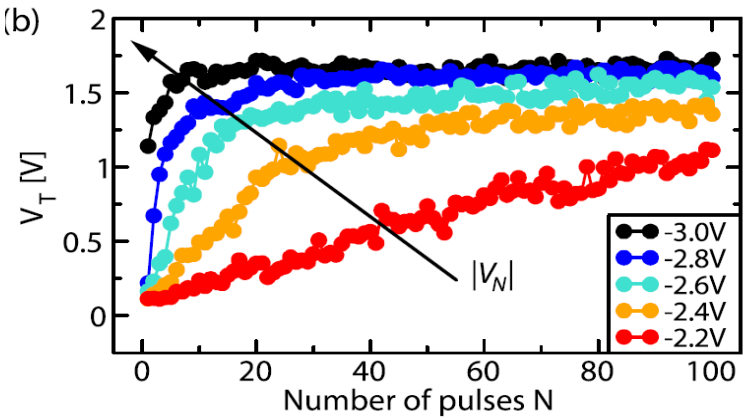






Accumulative Switching (AS)





- OSS and AS obey the universal time–voltage dependence ....

H. Mulaosmanovic, et al.
IEEE TED 67.12 (2020)

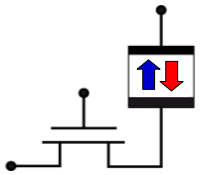
☑ Decent **linearity** has been demonstrated for FeFET

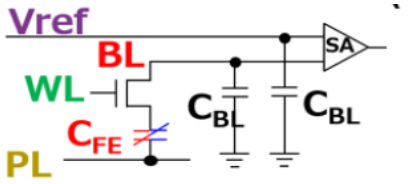
☑ Gradual switching needs multiple domains → **large devices**

Funded by the European Union

Scalability – Variability – On-currents in FeCAPs and FeFETs

FIXIT

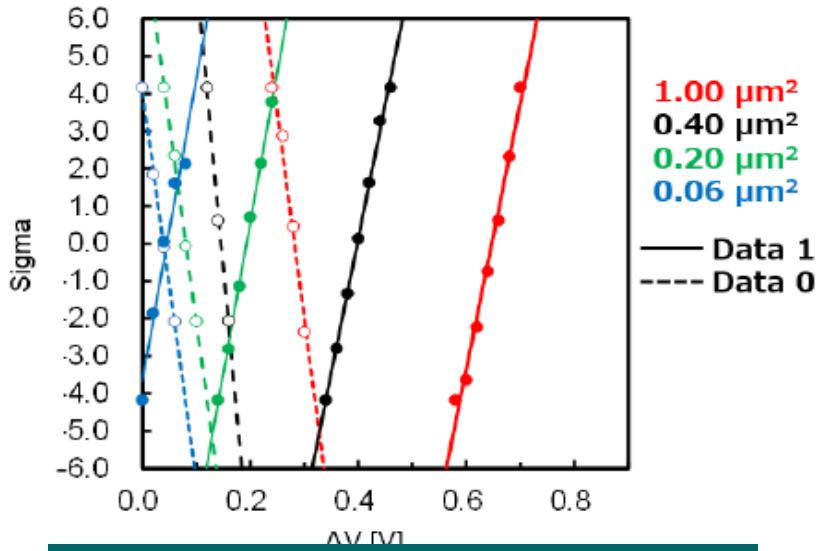




$$VBL = \frac{CFE}{(CFE + CBL)} \times VPL$$

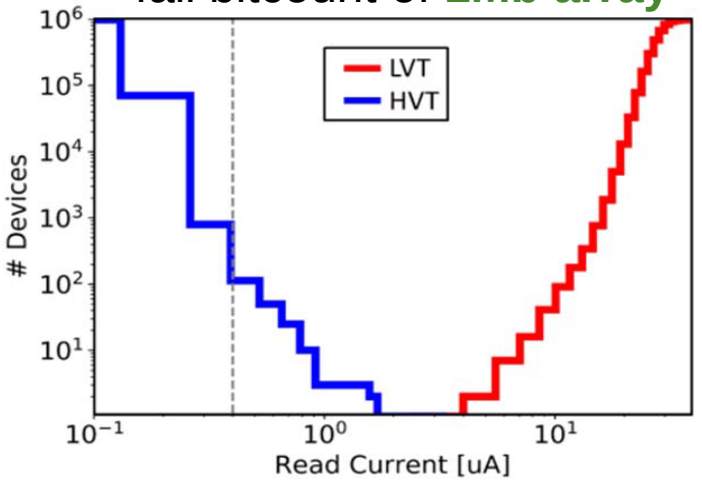
$CFE = C0$ or $C1$

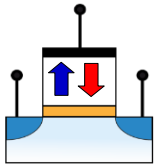
fail bitcount of **64kBit array**



J. Okuno et al., IMW 2021

fail bitcount of **1Mb array**





FeFET: L=450nm x W=450nm

-4.5V / +5V 10µs erase / program

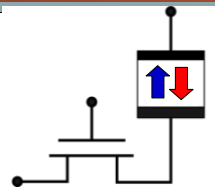
S. Beyer et al., IMW, 2020

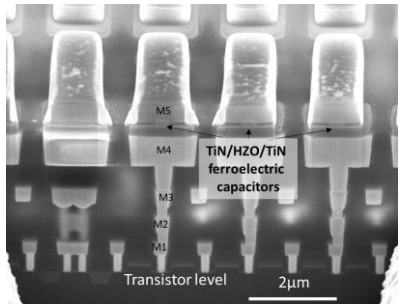
- **In FeCAPs :** ΔVBL depends on the capacitor area
- **In FeFETs** the on-current can be easily tuned by W/L ratio
- ☑ **FeFET / FeCAP memory arrays demonstrated (down to ~ 0.2 µm² device area)**
- For smaller devices stronger variability sets in due to poly-crystalline material

Funded by the European Union

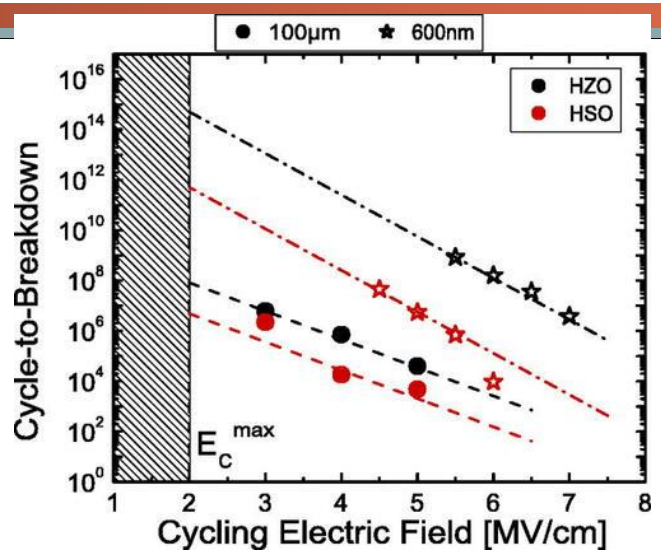
Cycling endurance

FIXIT

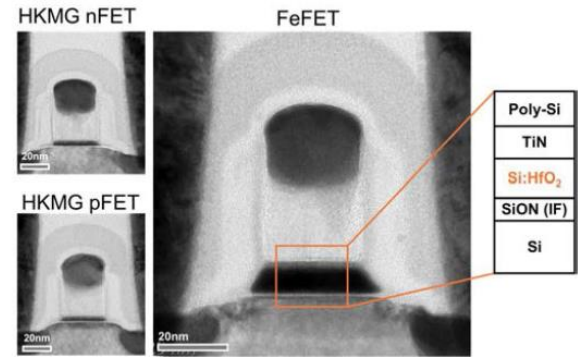




T. Francois et al., IEDM 2019



T. Francois et al., APL 2021

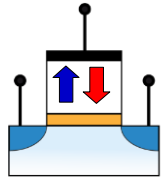


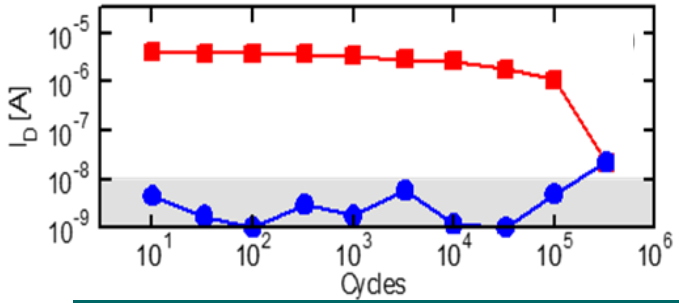
M. Trentzsch et al., IEDM 2016

S. Dünkel et al., IEDM 2017

Si: HfO_2 FeFET features:

- 10 nm polycrystalline HfO_2
- Memory window > 1V
- Retention > 10 years
- **Endurance: 10^4 –10^5**





H. Mulaosmanovic et al., TED 2019

☑ FeCAPs show superior endurance behaviour

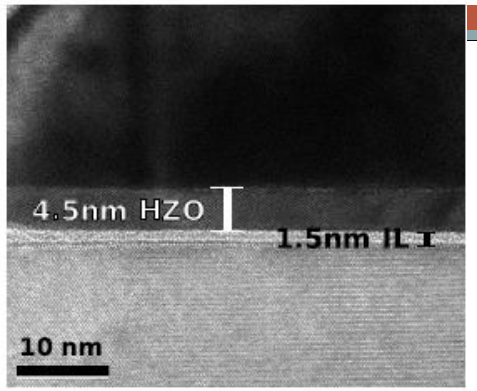
☑ FeFETs endurance is limited by the degradation of the interface dielectric

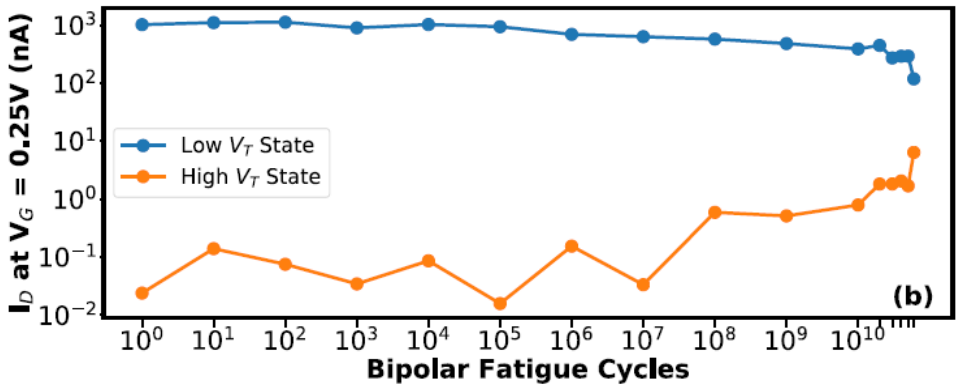
➢ Similar in double layer FTJ due to similar material stack

Funded by the European Union

Cycling endurance

FIXIT

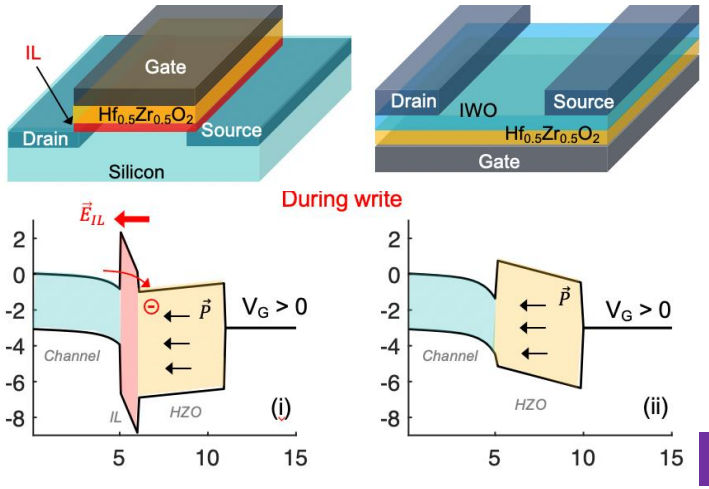


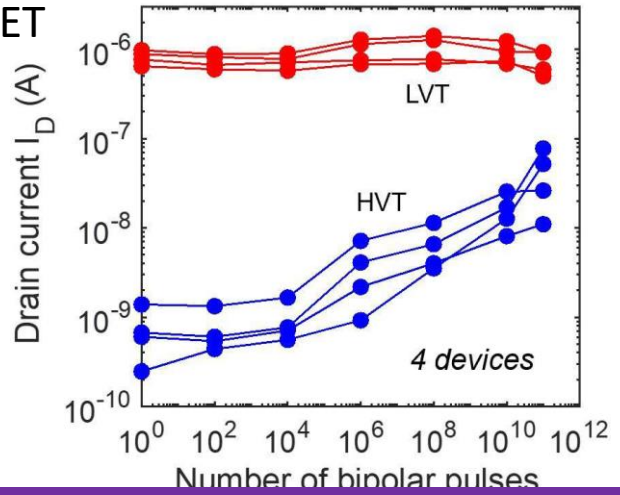


AJ. Tan et al., EDL 2021

☑ **Interfacial layer engineering** (high-k SiON) reduces field stress

convent. FeFET with IL IL-free IWO BEOL FeFET





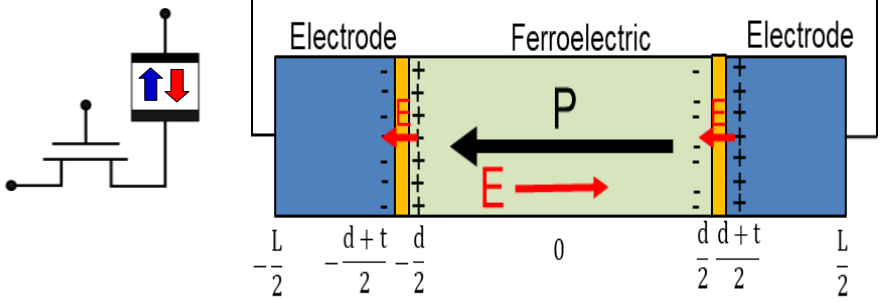
S. Dutta, et al., EDL 43.3, 382-385, (2022).

M. Halter et al., ACS Appl. Mater. Interfaces 2020

☑ Eliminating the interface in **BEOL compatible FeFETs** further improves cycling endurance

Funded by the European Union

Data retention



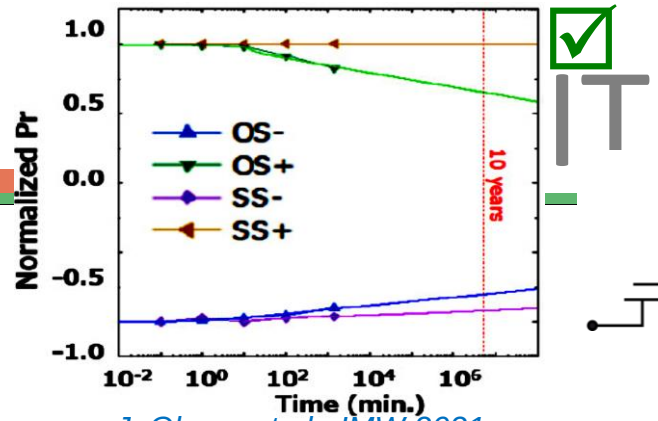
P. D. Lomenzo et al., NVMTS 2019
P. D. Lomenzo et al., ACS Appl. El. Mat. 2020
P. D. Lomenzo et al., APL 2020

Depolarization Field

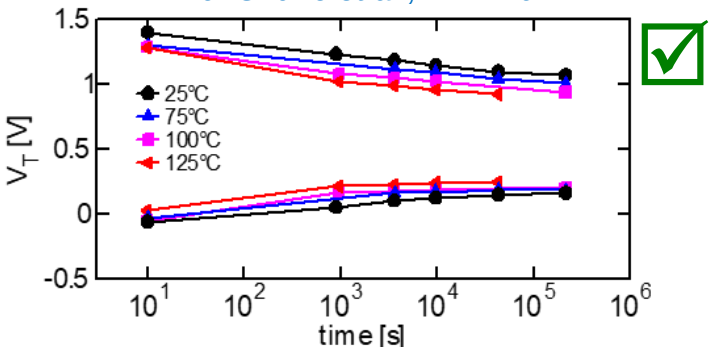
$$E_{FE} = \frac{-P d_{int}}{\varepsilon_0 (d_{int}\varepsilon_{FE} + d_{FE}\varepsilon_{int})}$$

Interface Field

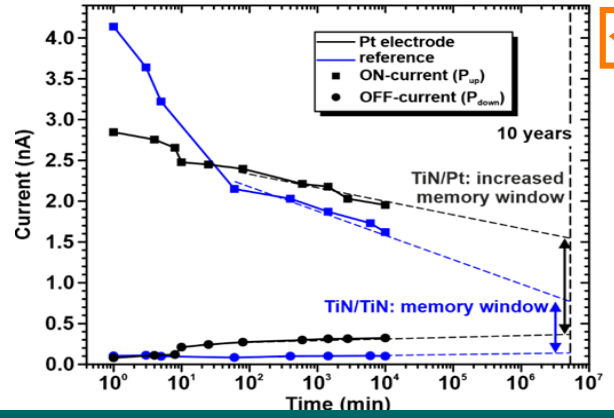
$$E_{INT} = \frac{P d_{FE}}{\varepsilon_0 (d_{int}\varepsilon_{FE} + d_{FE}\varepsilon_{int})}$$



J. Okuno et al., IMW 2021



H. Mulaosmanovic et al., TED 2020



B. Max et al., Electronics Letters 2020

- ☑ 10 year data retention for FeFET and FeCAP
  - ➢ Non ideal electrodes, non-polar regions lead to a depolarization field
  - ➢ In FeFETs and FTJs the interfacial layer increases the depolarization field

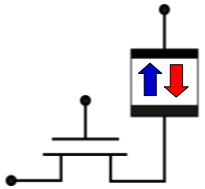
Funded by the European Union

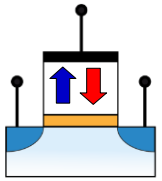
- Introduction
- Ferroelectric devices
  - Ferroelectric capacitor - FeCAP (for FeRAM)
  - Ferroelectric Field Effect Transistor - FeFET
  - Ferroelectric Tunneling Junction - FTJ
- Ferroelectrics for unconventional computing
- **Ferroelectric device comparison**
- Conclusion

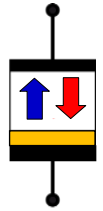
Funded by the European Union

Device comparison

FIXIT







	FeCAP	FeFET	FTJ
Non-volatility / data retention	✓	✓	✓
Programming voltages	✓	✓	✓
Non-destructive readout	✗	✓	✓
Cycling endurance	✓	✓	✓
Multi-level / analog switching	✓	✓	✓
Static read on-currents	✗	✓	✓
Fine-grained implementation	✓	✓	✓
Parallel operation	✓	✓	✓

Application

NVM

LiM / CiM / TCAM

CNN

Spiking

Edge inference

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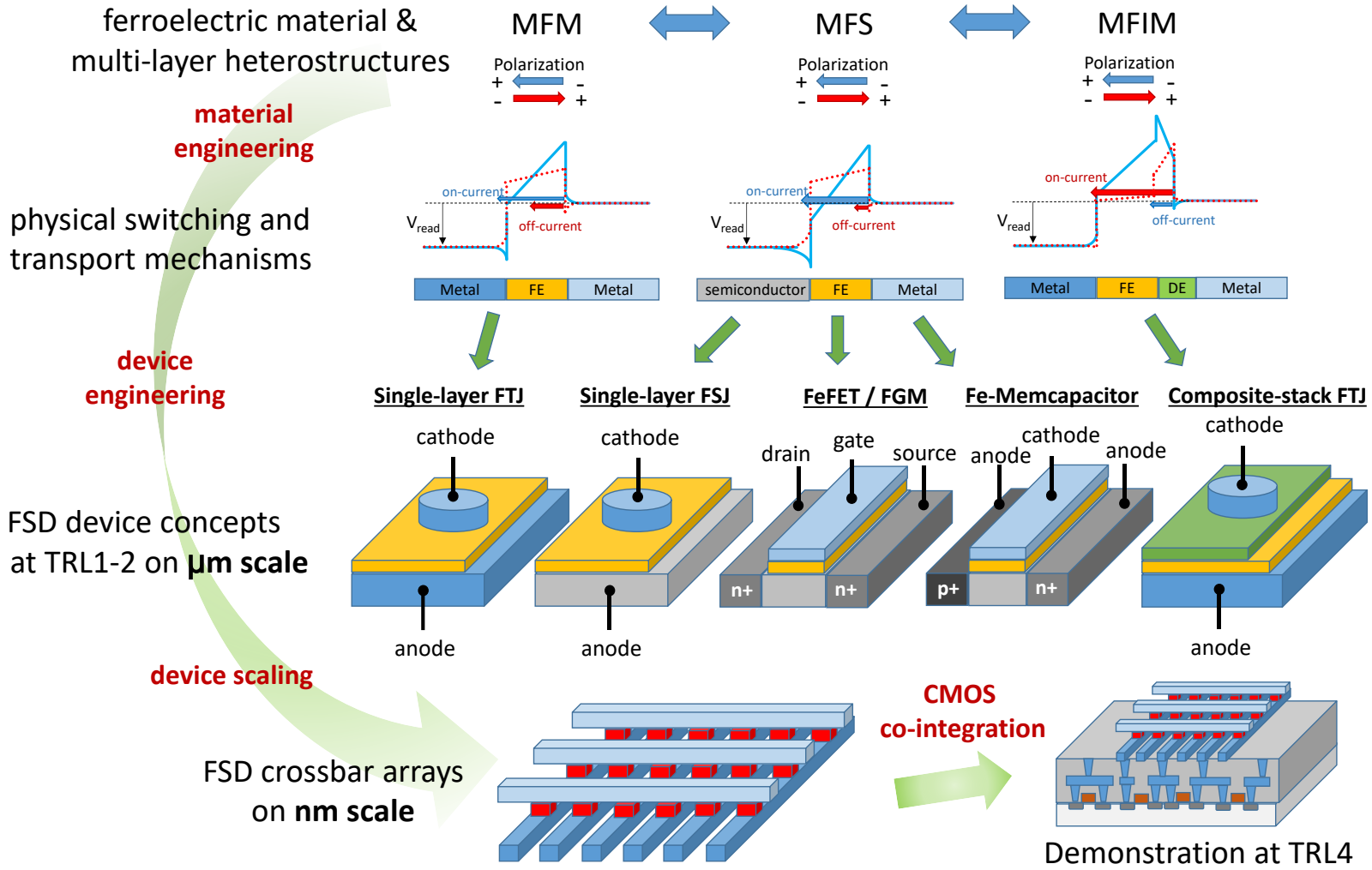
More FSD concepts…. The FIXIT project

FIXIT



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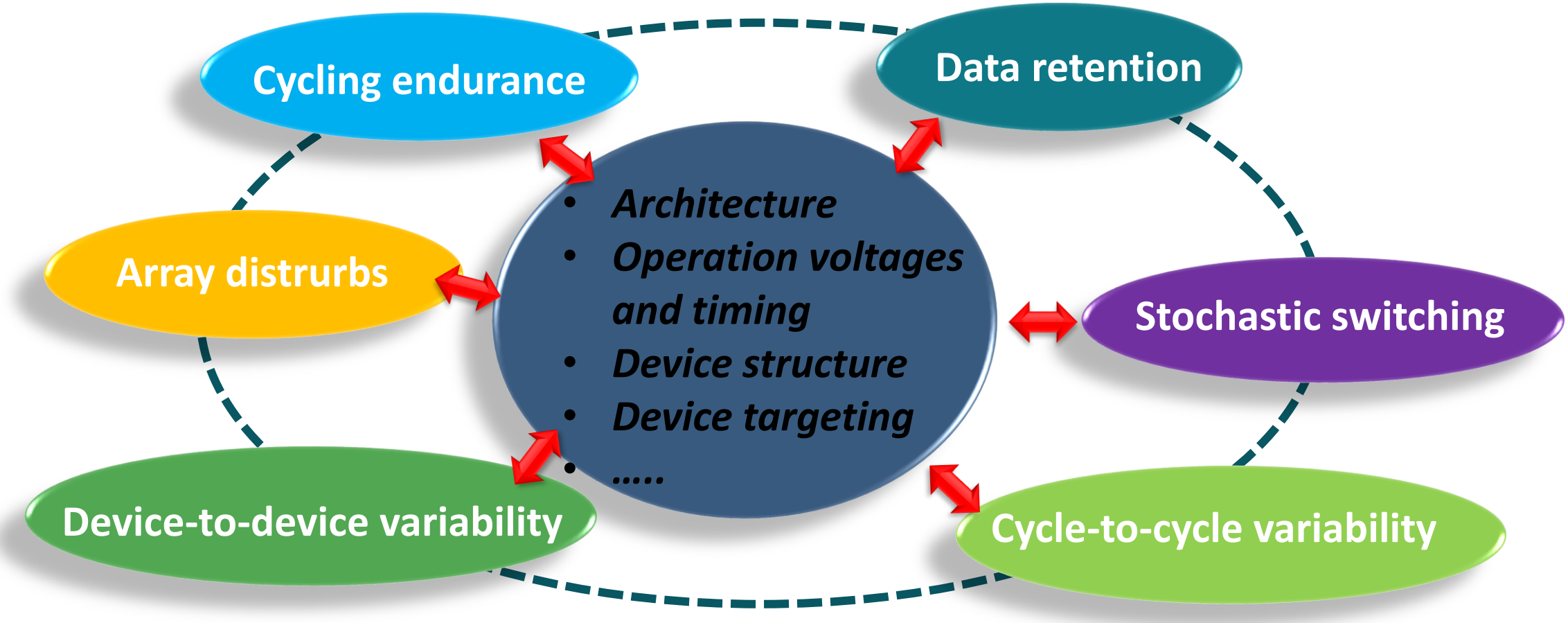
Summary and Conclusion

FIXIT



- There is a complex interplay between different reliability aspects of the ferroelectric devices that has to be tackled by thorough DTCO.

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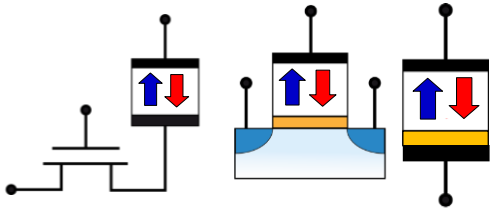
Conclusion

FIXIT



- HfO_2-based ferroelectric devices are getting mature
- Switching kinetics have strong impact on device operation
- FeCAP is best suited for memory application
- FeFET is the most versatile ferroelectric device
- FTJ is the most interesting device for parallel operation
- A thorough DTCO is mandatory to get the ferroelectric devices run

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THANK YOU!

QUESTIONS?

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